

MC1445
MC1545

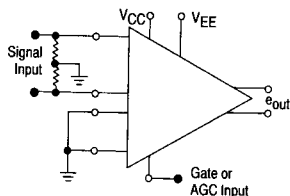
Gate Controlled Two Channel Input Wideband Amplifier

The MC1445/1545 was designed for use as a general purpose gated wideband amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier.

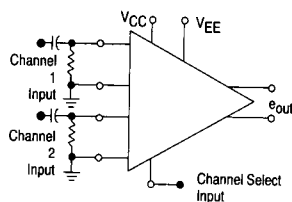
- Large Bandwidth; 50 MHz Typical
- Channel Select Time of 20 ns Typical
- Differential Inputs and Differential Output

Typical Applications

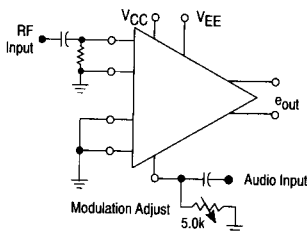
Video Switch or Differential Amplifier with AGC



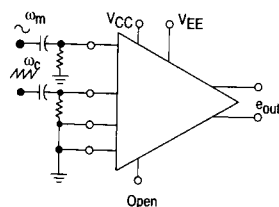
Multiplex or FSK



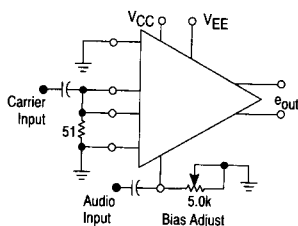
Amplitude Modulator



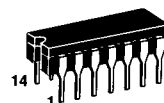
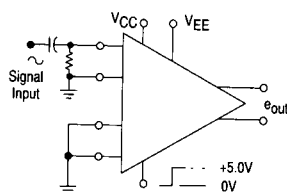
Pulse Width Modulator



Balanced Modulator

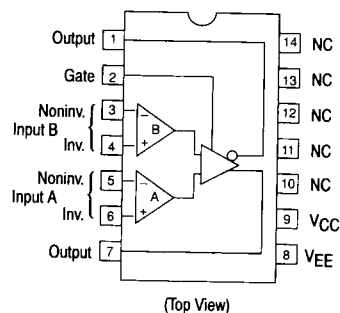


Analog Switch



L SUFFIX
CERAMIC PACKAGE
CASE 632

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
LM1445L	0° to +75°C	Ceramic DIP
LM1545L	-55° to +125°C	Ceramic DIP

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MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC} V _{EE}	+12 -12	Vdc
Input Differential Voltage Range	V _{IDR}	±5.0	V
Load Current	I _L	25	mA
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T _A = +25°C	P _D	625 5.0	mW mW/°C
Operating Ambient Temperature Range	MC1445 MC1545 T _A	0 to +75 -55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, @ T_A = +25°C, specifications apply to both input channels, unless otherwise noted.)

Characteristics	Fig. No.	Symbol	MC1545			MC1445			Unit
			Min	Typ	Max	Min	Typ	Max	
Single-Ended Voltage Gain	1, 12	A _{VS}	16	19	21	16	19.5	23	dB
Bandwidth	1, 12	BW	40	50	—	—	50	—	MHz
Input Impedance (f = 50 kHz)	5, 14	z _i	4.0	10	—	3.0	10	—	kΩ
Output Impedance (f = 50 kHz)	6, 15	z _o	—	25	—	—	25	—	Ω
Output Differential Voltage Range (R _L = 1.0 kΩ, f = 50 kHz)	4, 13	V _{ODR}	1.5	2.5	—	1.5	2.5	—	V _{p-p}
Input Bias Current	16	I _{IB}	—	15	25	—	15	30	μAdc
Input Offset Current	16	I _{IO}	—	2.0	—	—	2.0	—	μAdc
Input Offset Voltage	17	V _{IO}	—	1.0	5.0	—	—	7.5	mVdc
Quiescent Output dc Level	17	V _O	—	0.1	—	—	0.1	—	Vdc
Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V)	17	ΔV _O	—	±15	—	—	±15	—	mV
Common Mode Rejection (f = 50 kHz)	9, 18	CMR	—	85	—	—	85	—	dB
Input Common Mode Voltage Range	18	V _{ICR}	—	±2.5	—	—	±2.5	—	V _{pk}
Gate Characteristics Gate Input Voltage – Low Logic State (Note 1) Gate Input Voltage – High Logic State (Note 2)	8	V _{IL(G)} V _{IH(G)}	0.40 —	0.70 1.5	— 2.2	0.2 —	0.4 1.3	— 3.0	Vdc
Gate Input Current – Low Logic State (V _{IL(G)} = 0 V)	18	I _{IL(G)}	—	—	2.5	—	—	4.0	mA
Gate Input Current – High Logic State (V _{IH(G)} = +5.0 V)	18	I _{IH(G)}	—	—	2.0	—	—	4.0	μA
Step Response (e _{in} = 20 mV)	19	t _{PLH} t _{PHL} t _{TLH} t _{THL}	— — — —	6.5 6.3 6.5 7.0	10 10 15 15	— — — —	6.5 6.3 6.5 7.0	— — — —	ns
Wideband Input Noise (5.0 Hz – 10 MHz, R _S = 50 Ω)	10, 20	e _n	—	25	—	—	25	—	μV(rms)
DC Power Consumption	11, 20	P _C	—	70	110	—	70	150	mW

NOTES: 1. V_{IL(G)} is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
2. V_{IH(G)} is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

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Figure 1. Single-Ended Voltage Gain versus Frequency

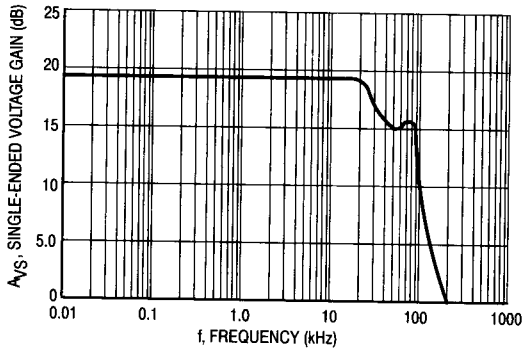


Figure 2. Single-Ended Voltage Gain versus Temperature

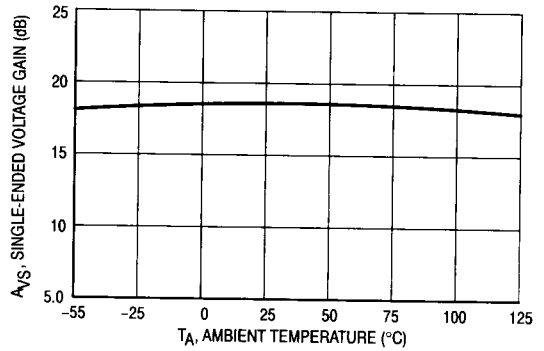


Figure 3. Voltage Gain versus Power Supply Voltages

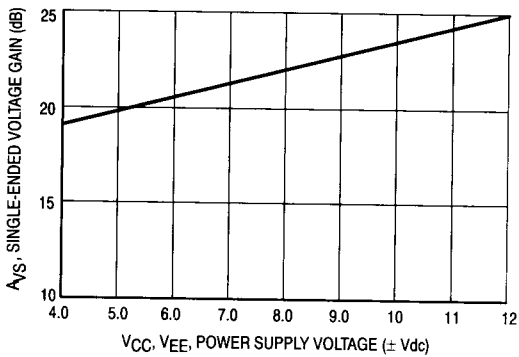


Figure 4. Output Voltage Swing versus Load Resistance

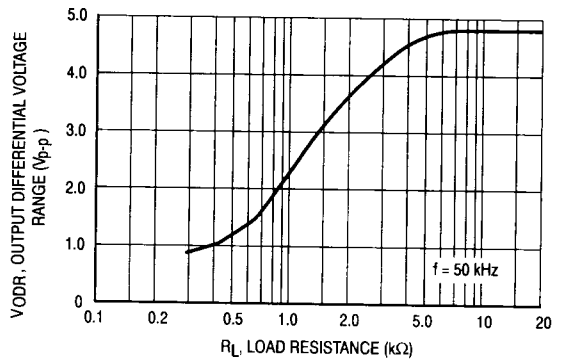


Figure 5. Input Cp and Rp versus Frequency (Both Channels)

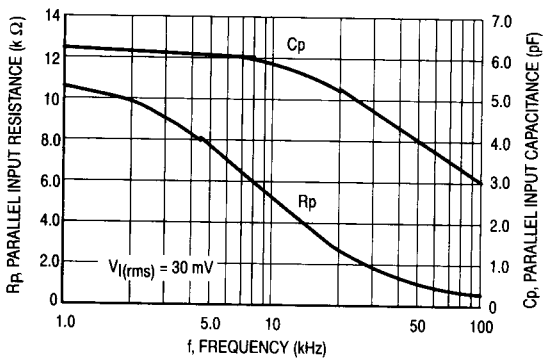
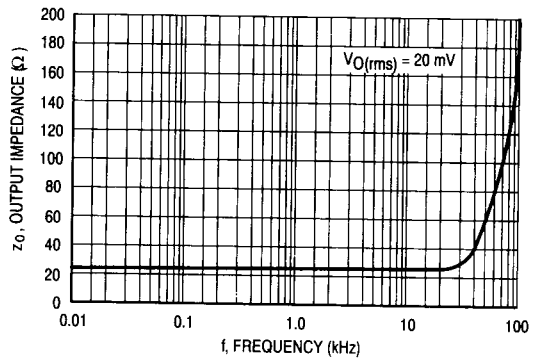


Figure 6. Output Impedance versus Frequency



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Figure 7. Channel Separation versus Frequency

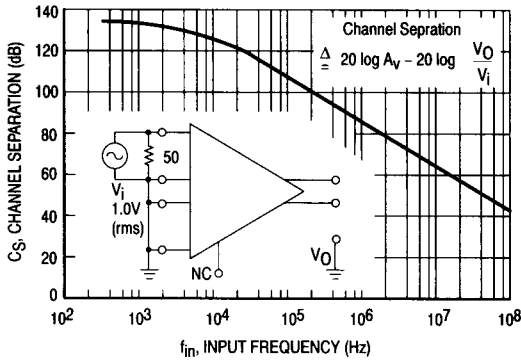


Figure 8. Gate Characteristics

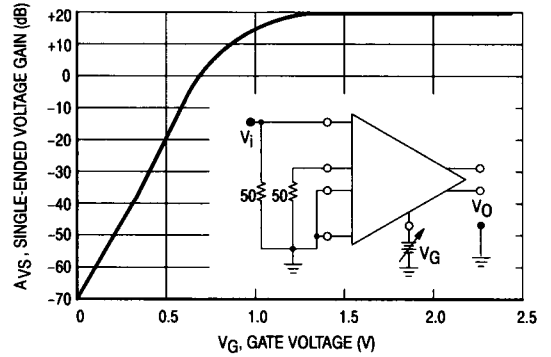


Figure 9. Common Mode Rejection Ratio versus Frequency

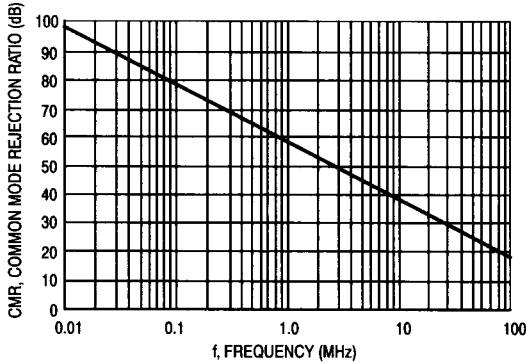


Figure 10. Input Wideband Noise versus Source Resistance

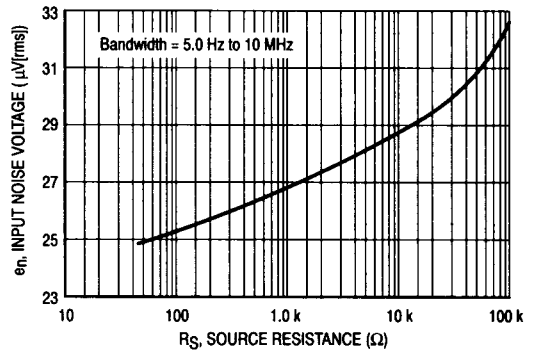


Figure 11. Circuit Schematic

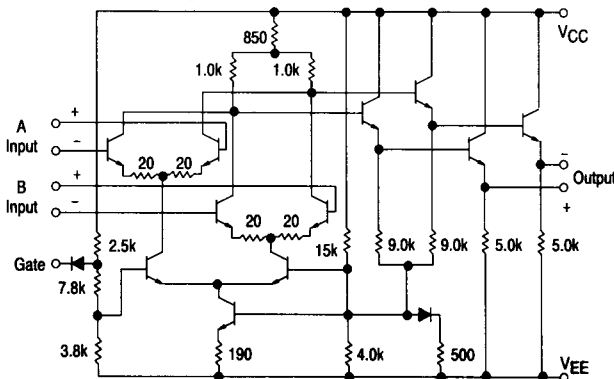
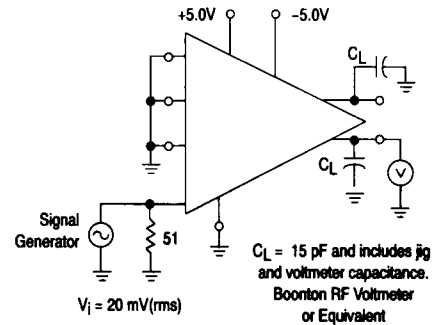


Figure 12. Single-Ended Voltage Gain and Bandwidth Test Circuit



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Figure 13. Output Voltage Swing Test Circuit

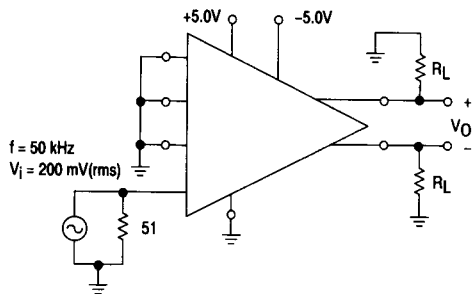


Figure 14. Input Impedance Test Circuit

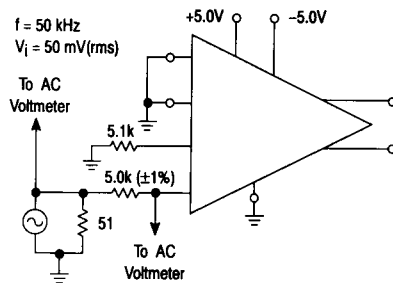


Figure 15. Output Impedance Test Circuit

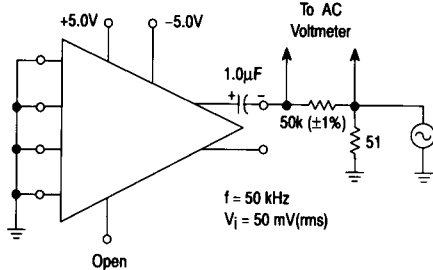


Figure 16. Input Bias Current and Input Offset Current Test Circuit

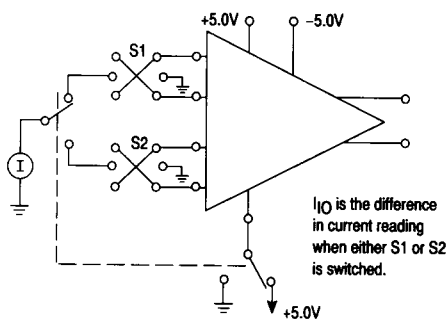


Figure 17. Input Offset Voltage and Quiescent Output Level Test Circuit

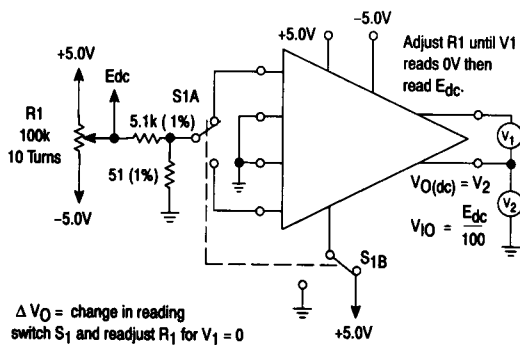
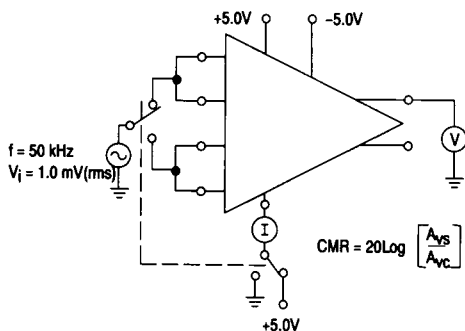


Figure 18. Gate Current (High and Low), Common Mode Rejection and Common Mode Input Range Test Circuit



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Figure 19. Propagation Delay, Rise and Fall Times Test Circuit

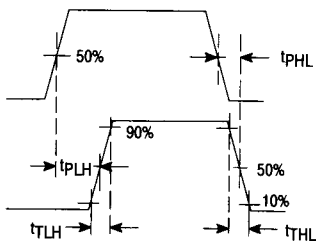
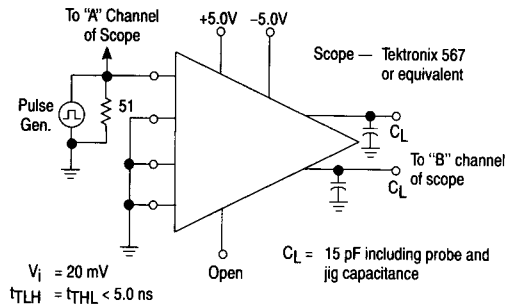


Figure 20. Power Dissipation and Wideband Input Noise Test Circuit

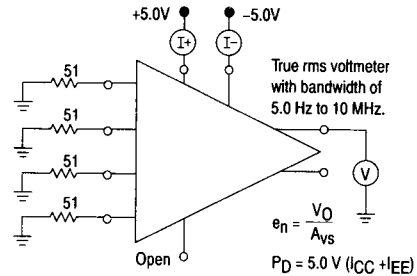


Figure 21. Limiting Characteristic

