SBOS377A – OCTOBER 2006 – REVISED FEBRUARY 2007

1.1nV/√Hz Noise, Low Power, Precision Operational Amplifier in Tiny DFN-8 Package

FEATURES

- **LOW-VOLTAGE NOISE: 1.1nV/√Hz at 1kHz**
- **100nV$_{PP}$ INPUT VOLTAGE NOISE, 0.1Hz–10Hz**
- **LOW OFFSET VOLTAGE: 100μV (max)**
- **LOW OFFSET VOLTAGE DRIFT: 0.2μV/°C (typ)**
- **LOW SUPPLY CURRENT: 3.6mA/Ch**
- **UNITY GAIN STABLE**
- **GAIN BANDWIDTH PRODUCT: 80MHz (G = 100)**
- **SLEW RATE: 27V/μs**
- **WIDE SUPPLY RANGE: ±2.25V to ±18V, +4.5V to +36V**
- **RAIL-TO-RAIL OUTPUT**
- **OUTPUT CURRENT: 30mA**
- **SHUTDOWN: 20μA (max)**
- **AVAILABLE IN TINY DFN-8 (3x3mm), MSOP-8, SO-8**

APPLICATIONS

- **PLL LOOP FILTER**
- **LOW-NOISE, LOW-POWER SIGNAL PROCESSING**
- **HIGH-PERFORMANCE ADC DRIVERS**
- **HIGH-PERFORMANCE DAC OUTPUT AMPLIFIER**
- **ACTIVE FILTERS**
- **LOW-NOISE INSTRUMENTATION AMPS**
- **ULTRASOUND AMPLIFIERS**
- **PROFESSIONAL AUDIO PREAMPLIFIERS**
- **LOW-NOISE FREQUENCY SYNTHESIZERS**
- **INFRARED DETECTOR AMPLIFIERS**
- **HYDROPHONE AMPLIFIERS**
- **MEDICAL**

DESCRIPTION

The OPA211 series achieves very low 1.1nV/√Hz noise density with a supply current of only 3.6mA. It also offers rail-to-rail output swing, which helps to maximize dynamic range.

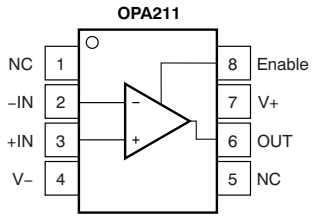
The OPA211 series' extremely low voltage and current noise, high speed and wide output swing make it an excellent choice as a loop filter amplifier in PLL applications.

In precision data acquisition applications, the OPA211 series of op amps provide <1μs settling time to 16-bit accuracy even for 10V output swings. This ac performance, combined with only 100μV of offset and low drift over temperature, make the OPA211 highly suitable for driving fast, high-precision analog-to-digital converters (ADCs) or buffering the outputs of high-resolution digital-to-analog converters (DACs).

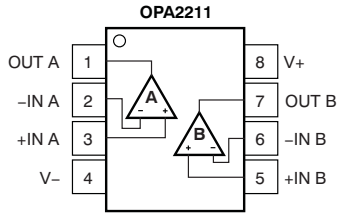
The OPA211 is specified over the very wide dual-power supply range of ±2.25V to ±18V, or single-supply operation from +4.5V to +36V.

The OPA211 is available in the tiny DFN-8 (3×3mm) and MSOP-8 and SO-8 packages. A dual version, the OPA2211, is available in the DFN-8 (3×3mm) or an MSOP-8 package. This series of op amps is specified from –40°C to +125°C.

PRODUCT PREVIEW



MSOP-8



MSOP-8

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Supply Voltage	±20	V
Input Voltage	(V–) – 0.7 to (V+) + 0.7	V
Input Current	±10	mA
Output Short-Circuit(2)	Continuous	
Operating Temperature	–55 to +150	°C
Storage Temperature	–65 to +150	°C
Junction Temperature	+150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to ground, one amplifier per package.

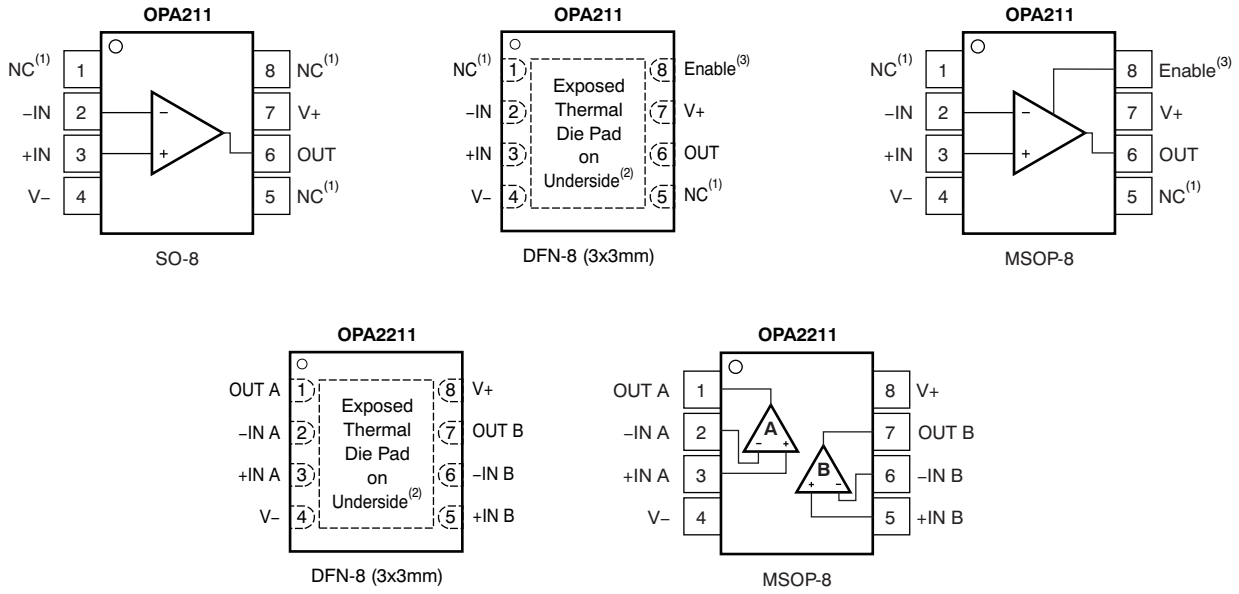
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	SINGLE	ENABLE	DUAL	PACKAGE DESIGNATOR	PACKAGE MARKING
Standard Grade						
OPA211A	DFN-8 (3×3mm)(2)	ü	ü		DRG	TBD
	MSOP-8(2)	ü	ü		DCK	TBD
OPA211A	SO-8	ü			D	TBD
OPA2211A	DFN-8 (3×3mm)(2)			ü	DRG	TBD
	MSOP-8(2)			ü	DCK	TBD
High Grade						
OPA211I	DFN-8 (3×3mm)(2)	ü	ü		DRG	TBD
	MSOP-8(2)	ü	ü		DCK	TBD
	SO-8	ü			D	TBD
OPA2211I	DFN-8 (3×3mm)(2)			ü	DRG	TBD
	MSOP-8(2)			ü	DCK	TBD

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Available Q4, 2007.

PRODUCT PREVIEW

PIN CONFIGURATIONS



(1) NC denotes no internal connection. Pin can be left floating or connected to any voltage between (V–) and (V+).
(2) Connect thermal die pad to V–.
(3) Enable function: (V–) ≤ ENABLED ≤ (V+) – 3V; DISABLED ≥ (V+) – 0.35V.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V

BOLDFACE limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA211A, OPA2211A			High Grade OPA211I, OPA2211I(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}	±15V		±20	±100		±20	TBD	µV
Drift	**dV_{OS}/dT**			**0.35**	**1**		**0.35**		**µV/°C**
vs Power Supply	**PSRR**	**V_S = ±2.25V to ±18V**			**2**			TBD	**µV/V**
INPUT BIAS CURRENT									
Input Bias Current	I_B	V_{CM} = 0V		30	150		30	TBD	nA
Over Temperature				**TBD**	**TBD**		**TBD**	**TBD**	**nA**
Offset Current	I_{OS}	V_{CM} = 0V		10	100		10	TBD	nA
Over Temperature				**TBD**	**TBD**		**TBD**	**TBD**	**nA**
NOISE									
Input Voltage Noise:	e_n								
f = 0.1Hz to 10Hz				0.1			0.1		μV_{PP}
Voltage Noise Density:									
f = 10Hz				2.5			2.5		$nV/\sqrt{Hz}$
f = 100Hz				1.6			1.6		$nV/\sqrt{Hz}$
f = 1kHz				1.1			1.1		$nV/\sqrt{Hz}$
Input Current Noise Density:	i_n								
f = 10Hz				TBD			TBD		$pA/\sqrt{Hz}$
f = 1kHz				1.5			1.5		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}		(V–)+1.8		(V+)–1.4	(V–)+1.8		(V+)–1.4	V
Common-Mode Rejection Ratio	CMRR	(V–)+1.8V < V_{CM} < (V+)–1.4V	114	120		114	120		dB
INPUT IMPEDANCE									
Differential				10^{10}||TBD			10^{10} ||TBD		Ω || pF
Common-Mode				10^9|| 2			10^9 || 2		Ω || pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	**A_{OL}**	**(V–)+0.2V < V_O < (V+)–0.2V, R_L = 10kΩ**	**114**	**120**		**114**	**120**		**dB**
	A_{OL}	(V–)+0.6V < V_O < (V+)–0.6V, R_L = 600Ω	110	114			114		dB
Over Temperature		**(V–)+0.6V < V_O < (V+)–0.6V, R_L = 600Ω, I_O < 25mA**	**110**	**114**		**110**	**114**		**dB**
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW	G = 100		80			80		MHz
		G = 1		58			58		MHz
Slew Rate	SR			27			27		V/µs
Settling Time, 0.01%	t_S	G = –1, 10V Step, C_L = 100pF		TBD			TBD		µs
0.0015% (16-bit)		G = –1, 10V Step, C_L = 100pF		TBD			TBD		µs
Overload Recovery Time		G = –1		< 1			< 1		µs
Total Harmonic Distortion + Noise	THD+N	G = +10, f = 20kHz, V_O = $20V_{PP}$, 600Ω		TBD			TBD		%

(1) **Shaded cells** indicate different specifications from low-grade version of device.

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V (continued)

BOLDFACE limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA211A, OPA2211A			High Grade OPA211I, OPA2211I[1]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT									
Voltage Output	**V_{OUT}**	**R_L = 10kΩ, A_{OL} > 114dB**	**(V–)+0.2**		**(V+)–0.2**	**(V–)+0.2**		**(V+)–0.2**	**V**
		R_L = 600Ω, A_{OL} > 110dB	(V–)+0.6		(V+)–0.6	(V–)+0.6		(V+)–0.6	V
		R_L = 600Ω, A_{OL} > 110dB, I_O < 25mA	**(V–)+0.6**		**(V+)–0.6**	**(V–)+0.6**		**(V+)–0.6**	**V**
Short-Circuit Current	I_{SC}			+30/–45			+30/–45		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			See Typical Characteristics			pF
POWER SUPPLY									
Specified Voltage	V_S		±2.25		±18	±2.25		±18	V
Quiescent Current (per channel)	I_Q	I_{OUT} = 0		3.6	TBD		3.6	TBD	mA
Over Temperature				**TBD**	**TBD**		**TBD**	**TBD**	**mA**
Shutdown Current		Disabled		TBD	20		TBD	20	µA
ENABLE Pin Input Voltage		Enabled			(V+)–3			(V+)–3	V
ENABLE Pin Input Voltage		Disabled	(V+)–0.35			(V+)–0.35			V
TEMPERATURE RANGE									
Specified Range			–40		+125	–40		+125	°C
Operating Range			–55		+150	–55		+150	°C
Thermal Resistance	θ_{JA}								
DFN (3mm × 3mm)		Soldered to approximately 5cm × 5cm copper area		65			65		°C/W
SO-8, MSOP-8				150			150		°C/W

PRODUCT PREVIEW

PACKAGING INFORMATION

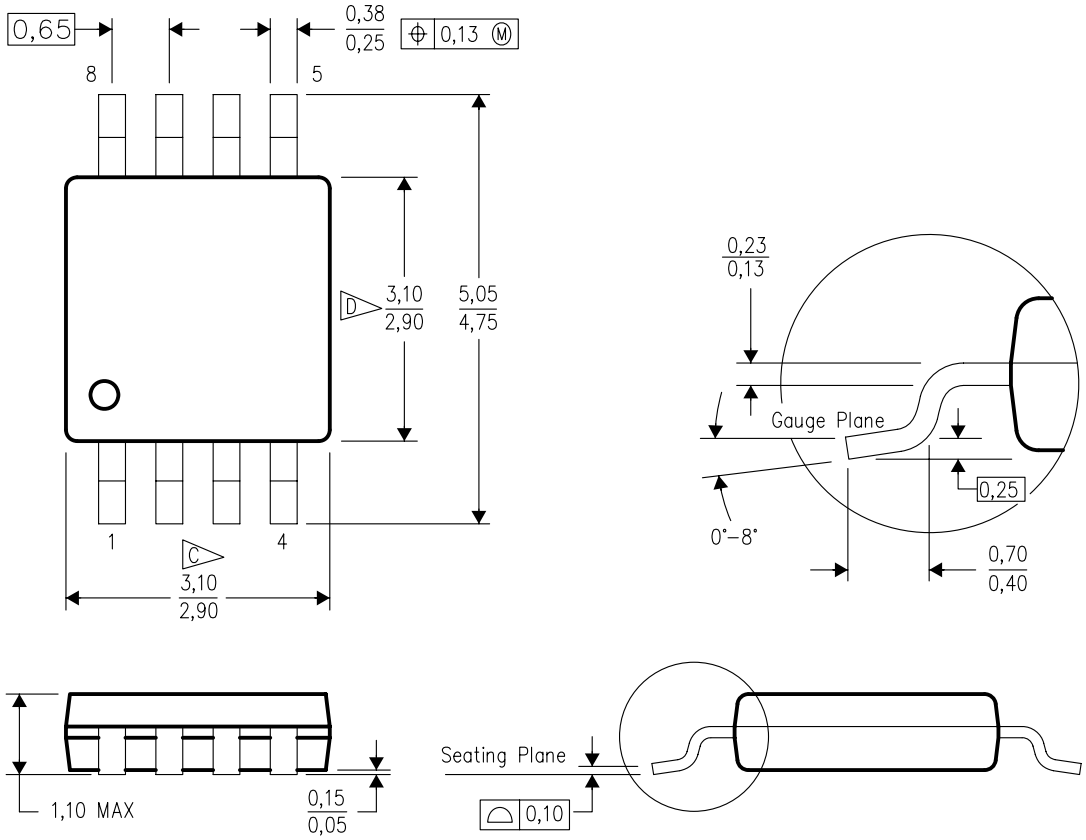
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA211AID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI
OPA211AIDGKR	PREVIEW	MSOP	DGK	8	2500	TBD	Call TI	Call TI
OPA211AIDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI
OPA211AIDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI
POPA211AID	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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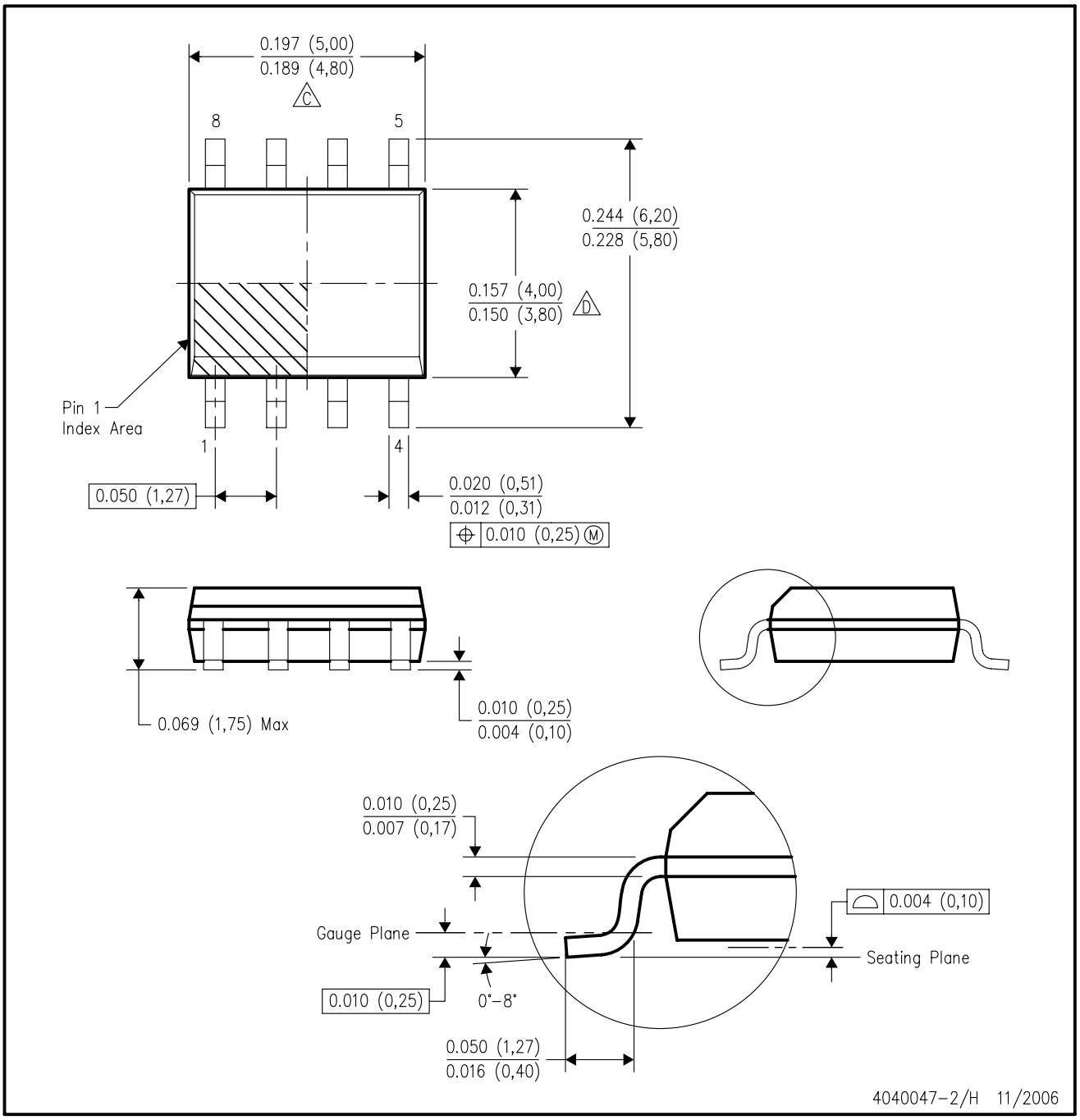
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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