

TL182, TL185, TL188, TL191 BI-MOS SWITCHES

D2234, JUNE 1976—REVISED SEPTEMBER 1986

- Functionally Interchangeable with Siliconix DG182, DG185, DG188, DG191 with Same Terminal Assignments
- Monolithic Construction
- Adjustable Reference Voltage
- JFET Inputs
- Uniform On-State Resistance for Minimum Signal Distortion
- $\pm 10\text{-V}$ Analog Voltage Range
- TTL, MOS, and CMOS Logic Control Compatibility

description

The TL182, TL185, TL188, and TL191 are monolithic high-speed analog switches using BI-MOS technology. They comprise JFET-input buffers, level translators, and output JFET switches. The TL182 switches are SPST; the TL185 switches are SPDT. The TL188 is a pair of complementary SPST switches as is each half of the TL191.

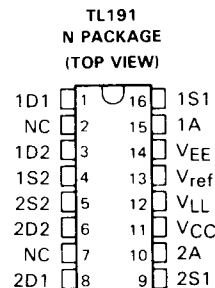
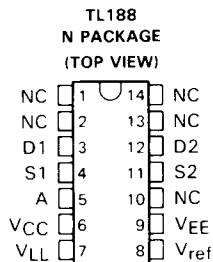
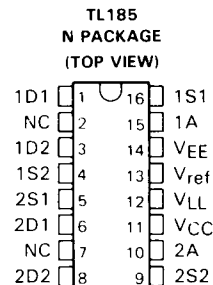
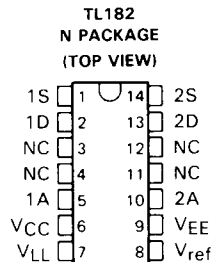
A high level at a control input of the TL182 turns the associated switch off. A high level at a control input of the TL185 turns the associated switch on. For the TL188, a high level at the control input turns the associated switches S1 on and S2 off.

The threshold of the input buffer is determined by the voltage applied to the reference input (V_{ref}). The input threshold is related to the reference input by the equation $V_{th} = V_{ref} + 1.4\text{ V}$. Thus, for TTL compatibility, the V_{ref} input is connected to ground. The JFET input makes the device compatible with bipolar, MOD, and CMOS logic families. Threshold compatibility may, again, be determined by $V_{th} = V_{ref} + 1.4\text{ V}$.

The output switches are junction field-effect transistors featuring low on-state resistance and high off-state resistance. The monolithic structure ensures uniform matching.

BI-MOS technology is a major breakthrough in linear integrated circuit processing. BI-MOS can have ion-implanted JFETs, p-channel MOS-FETs, plus the usual bipolar components all on the same chip. BI-MOS provides for monolithic circuit designs that previously have been available only as expensive hybrids.

M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C . I-suffix devices are characterized for operation from -25°C to 85°C , and C-suffix devices are characterized for operation from 0°C to 70°C .



NC—No internal connection

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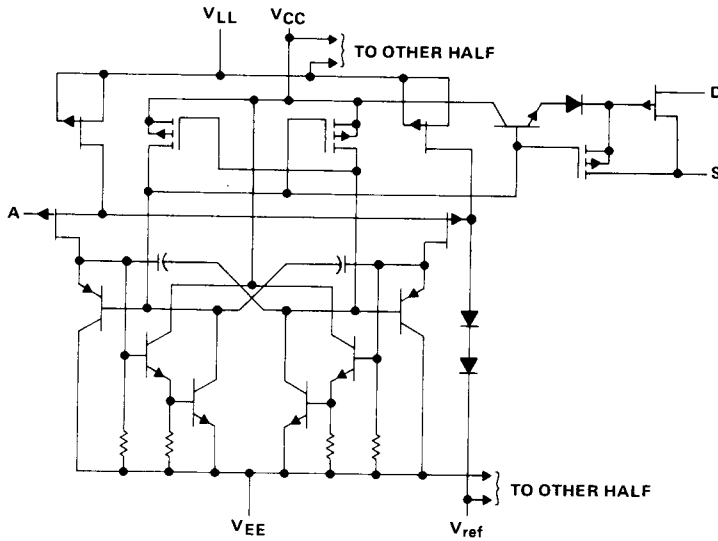
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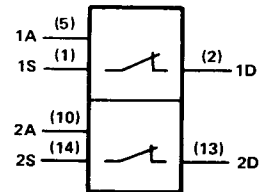
TL182, TL185 **BI-MOS SWITCHES**

TL182 TWIN SPST SWITCH

schematic (each channel)



symbol

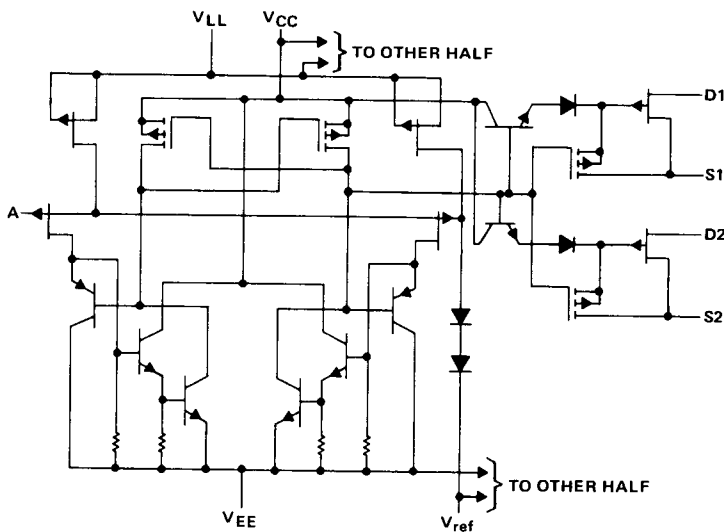


FUNCTION TABLE
(EACH HALF)

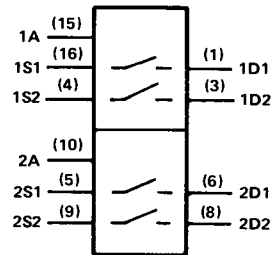
INPUT A	SWITCH S
L	ON (CLOSED)
H	OFF (OPEN)

TL185 TWIN DPST SWITCH

schematic (each channel)



symbol

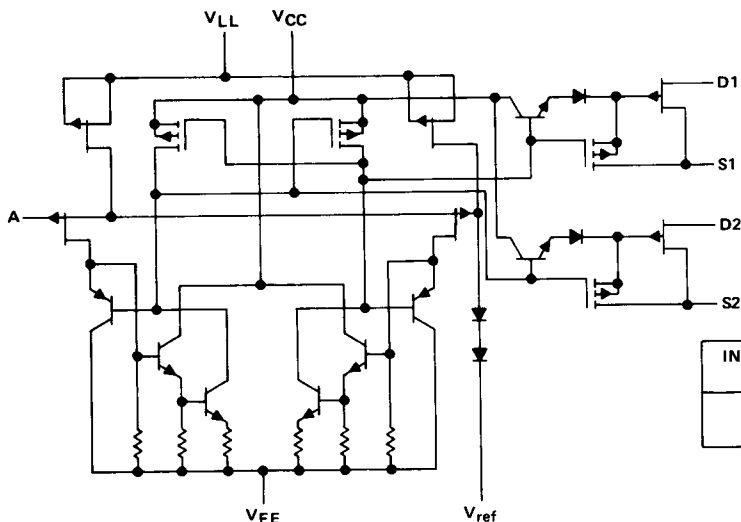


FUNCTION TABLE
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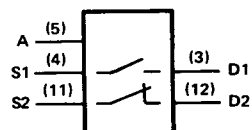
INPUT A	SWITCHES SW1 AND SW2
L	OFF (OPEN)
H	ON (CLOSED)

TL188 DUAL COMPLEMENTARY SPST SWITCH

schematic



symbol

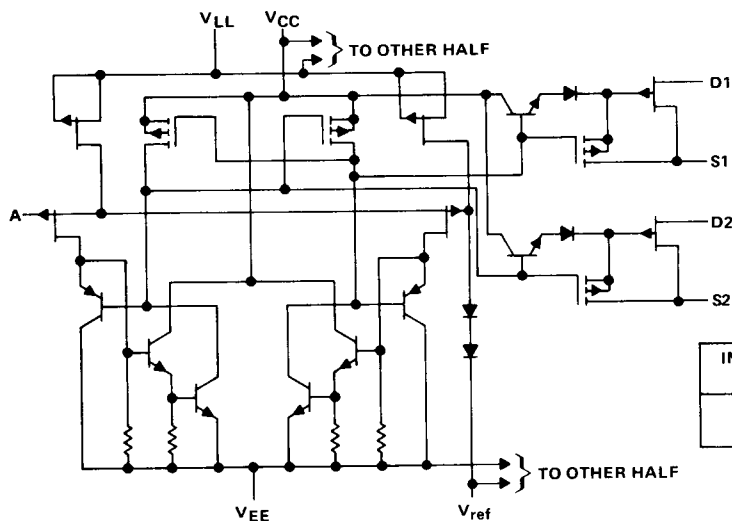


FUNCTION TABLE

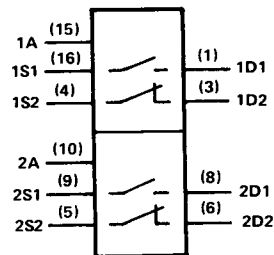
INPUT A	SWITCHES	
	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

TL191 TWIN DUAL COMPLEMENTARY SPST SWITCH

schematic (each channel)



symbol



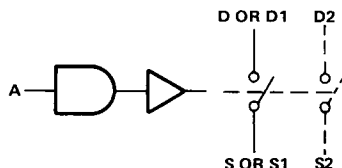
FUNCTION TABLE

INPUT A	SWITCHES	
	SW1	SW2
L	OFF (OPEN)	ON (CLOSED)
H	ON (CLOSED)	OFF (OPEN)

TL182, TL185, TL188, TL191

BI-MOS SWITCHES

functional block diagram



See the preceding two pages for operation of the switches.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply to negative supply voltage, $V_{CC} - V_{EE}$	36 V
Positive supply voltage to either drain, $V_{CC} - V_D$	33 V
Drain to negative supply voltage, $V_D - V_{EE}$	33 V
Drain to source voltage, $V_D - V_S$	± 22 V
Logic supply to negative supply voltage, $V_{LL} - V_{EE}$	36 V
Logic supply to logic input voltage, $V_{LL} - V_I$	33 V
Logic supply to reference voltage, $V_{LL} - V_{ref}$	33 V
Logic input to reference voltage, $V_I - V_{ref}$	33 V
Reference to negative supply voltage, $V_{ref} - V_{EE}$	27 V
Reference to logic input voltage, $V_{ref} - V_I$	2 V
Current (any terminal)	30 mA
Operating free-air temperature range: TL182M, TL185M, TL188M, TL191M	-55°C to 125°C
TL182I, TL185I, TL188I, TL191I	-25°C to 85°C
TL182C, TL185C, TL188C, TL191C	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

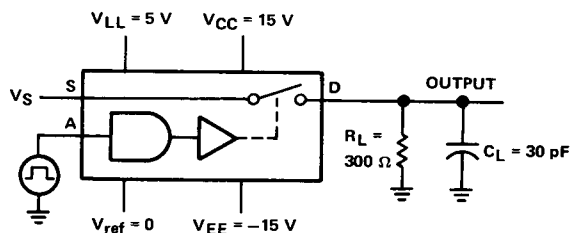
electrical characteristics, $V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$, $V_{LL} = 5\text{ V}$, $V_{ref} = 0\text{ V}$

PARAMETER	TEST CONDITIONS	TL1_M		TL1_I		TL1_C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level control input voltage	$T_A = \text{MIN TO MAX}$		$V_{ref} + 2$		$V_{ref} + 2$		V
V_{IL}	Low-level control input voltage	$T_A = \text{MIN TO MAX}$		$V_{ref} + 0.8$		$V_{ref} + 0.8$		V
I_{IH}	High-level control input current	$V_I = 5\text{ V}$		$T_A = 25^\circ\text{C}$		10		μA
I_{IL}	Low-level control input current	$V_I = 0$		$T_A = \text{MAX}$		20		μA
$I_{D(off)}$	Off-state drain current	$V_D = 10\text{ V}$, $V_S = -10\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$		$T_A = \text{MIN TO MAX}$		$V_{ref} + 0.8$		V
$I_{S(off)}$	Off-state source current	$V_D = -10\text{ V}$, $V_S = 10\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$		$T_A = \text{MAX}$		10		μA
$I_{D(on)} + I_{S(on)}$	On-state channel leakage current	$V_D = -10\text{ V}$, $V_S = -10\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$		$T_A = \text{MIN TO MAX}$		20		μA
$r_{DS(on)}$	Drain-to-source on-state resistance	$V_D = -10\text{ V}$, $I_S = 1\text{ mA}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$		$T_A = \text{MIN TO MAX}$		100		Ω
I_{CC}	Supply current from V_{CC}	$T_A = 25^\circ\text{C}$		$T_A = \text{MIN TO MAX}$		5		nA
I_{EE}	Supply current from V_{EE}	$T_A = 25^\circ\text{C}$		$T_A = \text{MAX}$		100		nA
I_{LL}	Supply current from V_{LL}	$T_A = 25^\circ\text{C}$		$T_A = \text{MIN TO MAX}$		5		nA
I_{ref}	Reference current	$T_A = 25^\circ\text{C}$		$T_A = \text{MAX}$		100		nA
I_{CC}	Supply current from V_{CC}	$T_A = 25^\circ\text{C}$		$T_A = \text{MIN TO MAX}$		100		nA
I_{EE}	Supply current from V_{EE}	$T_A = 25^\circ\text{C}$		$T_A = \text{MAX}$		150		nA
I_{LL}	Supply current from V_{LL}	$T_A = 25^\circ\text{C}$		$T_A = \text{MIN TO MAX}$		150		nA
I_{ref}	Reference current	$T_A = 25^\circ\text{C}$		$T_A = \text{MAX}$		300		nA
I_{CC}	Supply current from V_{CC}	$T_A = 25^\circ\text{C}$		$T_A = \text{MIN TO MAX}$		1.5		mA
I_{EE}	Supply current from V_{EE}	$T_A = 25^\circ\text{C}$		$T_A = \text{MAX}$		1.5		mA
I_{LL}	Supply current from V_{LL}	$T_A = 25^\circ\text{C}$		$T_A = \text{MIN TO MAX}$		1.5		mA
I_{ref}	Reference current	$T_A = 25^\circ\text{C}$		$T_A = \text{MAX}$		1.5		mA

switching characteristics, $V_{CC} = 10\text{ V}$, $V_{EE} = -20\text{ V}$, $V_{LL} = 5\text{ V}$, $V_{ref} = 0\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL1_M		TL1_I		TL1_C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	
t_{on}	$R_L = 300\ \Omega$, $C_L = 30\text{ pF}$, Figure 1	175	350	175	350	175	350	ns
t_{off}		175	350	175	350	175	350	ns

PARAMETER MEASUREMENT INFORMATION

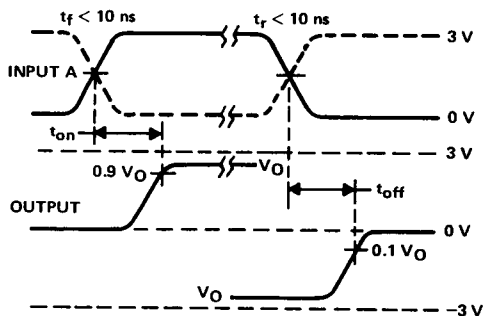


C_L includes probe and jig capacitance

$V_S = 3\text{ V}$ for t_{on} and -3 V for t_{off}

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

TEST CIRCUIT



NOTE: A. The solid waveform applies for TL185 and SW1 of TL185 and TL191; the dashed waveform applies for TL182 and SW2 of TL185 and TL191.

B. V_O is the steady-state output with the switch on. Feed through via the gate capacitance may result in spikes (not shown) at the leading and trailing edges of the output waveform.

FIGURE 1. VOLTAGE WAVEFORMS