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Application Note

AN- TDA 1684X

A Controller Family for Switch Mode Power Supplies
Supporting Low Power Standby and
Power Factor Correction (PFC)

Author: Peter Preller

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Power Conversion

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TDA 1684X:
A Controller Family for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction (PFC)

Application Notes

Issue 1.2

Peter Preller
Infineon Technologies AG
Power Semiconductors - Technical Marketing
Munich - Germany

Contents:

Type	Ordering Code	Package
TDA 16846	Q67000-A9377	P-DIP-14-3
TDA 16847	Q67000-A9378	P-DIP-14-3
TDA 16846G	Q67006-A9430	P-DSO-14-3
TDA 16847G	Q67006-A9412	P-DSO-14-3

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11.5.1999, Issue 1.1:
Chapter 12 added:
Standby Input Power of the 80 W Demoboard with TDA 16846

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Chapter 1: Extension of the text.
Chapter 2: Fig. 1a,b,c,d: Measured waveforms of drain voltage.
Chapter 3: Extension of the text.
Chapter 6: Addition of the pin 1 modification.
Chapter 10 : Extension of the text (remarks to some pins).
Chapter 13 added: New Application Circuits.

1. Functions and Applications Overview

The TDA 1684X is optimized to control flyback converters with or without Power Factor Correction (PFC with Charge Pump Circuit) in the power range from 1 W to more than 300 W. Typical applications are TV-, VCR- sets and SAT receivers, but the TDA 1684X also can be used in PC monitors in free running, fixed frequency or synchronized mode, and in industrial power supply applications.

To provide low power consumption at light loads, in free running mode this device reduces the switching frequency in small steps with decreasing load towards an adjustable minimum (e. g. 20 kHz in standby mode). Smooth operation is possible for the whole load range from full load to no load. The load dependent frequency behavior is also advantageous for the new operating modes in TV sets between normal mode and standby mode (only the horizontal driver stage is shutdown) and for the energy saving modes in monitors defined by the VESA- PC- standard.

A special anti jitter circuit is implemented to avoid continuous jumping between zero crossing signals when the operating frequency is decreasing. To lower the switching stresses of the power devices, the power transistor is always switched on at minimum voltage in the free running mode.

To reduce power dissipation in standby mode the TDA 1684X has a very low supply current and is designed for a high value series resistor. Regulation can be done by using the internal error amplifier or an opto coupler feedback. According to a new method of primary regulation only a voltage divider is necessary instead of an external rectifier circuit between the control winding of the transformer and the control input .

In the fixed switching frequency mode the frequency can be set above the lowest freerunning frequency (at max. load and min. mains voltage). When the load exceeds the point at which the fixed frequency period is equal to the freerunning period, the SMPS changes continuously from the fixed frequency mode into the freerunning mode and vice versa. In this way the maximum energy can be transferred across the transformer.

All Figures shown are specific to the TDA 16846/7. Note: For new applications the fast switching Cool MOS transistors are available. All BUZ- MOS FETs which are integrated in the circuit diagrams in this application notes can be replaced by appropriate Cool MOS transistors.

2. Function of the Anti Jitter Circuit

An important characteristic of the TDA 1684X is it´s load dependent frequency response for free running switched mode power supplies (SMPSs). This function allows it to control sinusoidal switched mode power supplies featuring a PFC charge pump circuit as well as provide a low power standby operation.

In order to ensure a high level of efficiency with light loads, the TDA 1684X reduces the frequency gradually as the load drops, by increasing the number of zero crossings omitted. Pauses occur between the end of the transformer reset and the beginning of the next switching cycle. This ensures optimum compatibility between the switched mode power supply frequency and the load, across the whole load range from the maximum load down to no load.

Fig. 1 shows the drain voltage waveforms of the power transistor for a free running SMPS under different loads. Fig. 2 shows the load dependent frequency behavior, which has been confirmed by measurement. The diagramms a), b), c), and d) in Fig. 1 correspond with the ranges a), b), c), and d) of the output power in Fig. 2. Figures 1a, 1b, 1c, 1d show the real picked up waveforms.

Diagram a) in Fig. 1 shows the drain voltage with a full load, where the first zero crossing of the transformer results in activation each time. If the load decreases, the frequency initially increases with the same curve profile, due to the decreasing pulse width. Finally, a point is reached where the TDA 1684X ignores the first zero crossing and switches on at the second zero crossing. The drain voltage is then shaped as shown in diagram b). The frequency has moved down by a specific amount in comparison with the waveform at a). Curve c) shows the drain voltage when the load is reduced further (two zero crossings omitted). Finally, curve d) shows the drain voltage when the load has been significantly reduced (several zero crossings omitted).

A special anti jitter circuit in the TDA 1684X ensures a degree of hysteresis, in order to avoid switching rapidly between period lengths and to ensure that the same number of zero crossings is omitted each time, when running under a constant load. Continuous changing of period lengths would not have any serious effects but would cause higher ripple at the output voltages and noise in the transformer.

The pulse diagram of Fig. 3 shows the operation of the anti jitter circuit. A shifted control voltage Vcon_s, derived from the internal control voltage Vcon, is used for determining the off time (from t1 to t6). Vcon_s lies within the range: Vcon * 0.8 <= Vcon_s <= Vcon. Vcon_s is controlled by the anti jitter circuit so that the crossing point t5 between the decreasing voltage V1 and the shifted control voltage Vcon_s is in the middle between 2 zero crossing signals (ZC2 and ZC3).

Fig. 4 shows the block diagram of the anti jitter circuit. Between the control voltage Vcon and Vcon_s a controlled voltage source VS1 is built in. VS1 is controlled by the voltage Vcs of the capacitor Cs: VS1 = 0.2 * Vcs. When the voltage Vcs becomes higher, the voltage VS1 becomes higher and the voltage Vcon_s becomes lower. Cs is charged by the current Ic and discharged by Id. Ic is produced by a current source CS1 which is controlled by the signal Vcs_up which comes from the output of the gate G5. Id is produced by a current source CS2 which is controlled by the signal Vcs_down which comes from the output of the gate G6. The inputs of G5 are the inverted output of the On Time Flipflop ONTF, the output of the Off Time Comparator OFTC and the inverted output of the Ringing Suppression Time Flipflop RSTF. The inputs of G6 are the output of RSTF and the output of the Ringing Suppression Time Comparator RSTC, which is latched in the Flipflop VOLF.

The amplitude of the pulsed current Ic is 2 times the amplitude of the pulsed current Id: Ic = 5.4 µA, Id = 2.7 µA. Cs has a capacitance of 65 pF. The voltage Vcs is constant, when the duration of the pulse Vcs_up is the half of the duration of the pulse Vcs_down. (Fig. 3). So when the control voltage

Vcon changes within a range of Vcon * 0.2, Vcon_s and t5 remain stable. The pulse Vcs_up begins at the crossing point t5 and ends at the next switch on time t6. The pulse Vcs_down begins at the time t2 when the rising voltage V3 at pin 3 exceeds the threshold 2.5 V. This is the threshold for shortening the ringing suppression time. Vcs_down ends at t3 when V1 has reached 3.5 V (end of ringing suppression time). Now the rule in the specification of TDA1684X is understandable (see specification page 7, “Off-Time Circuit OTC”) that the ringing suppression time TC1, exactly the time t3 - t2 (more steep part of the rising voltage V1 between t1 and t3), should be as long as the period TR of the transformer oscillations. Then the cross-over point t5 is exactly in the middle between 2 zero crossing signals. Control range and noise sensitivity of the anti jitter circuit are well adjusted.

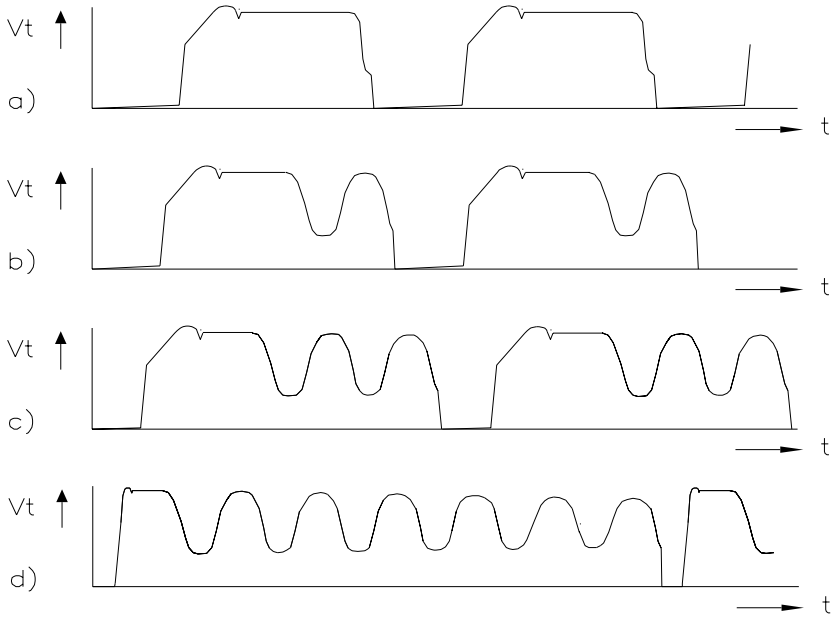

Fig. 1: Drainvoltage Vt at different load

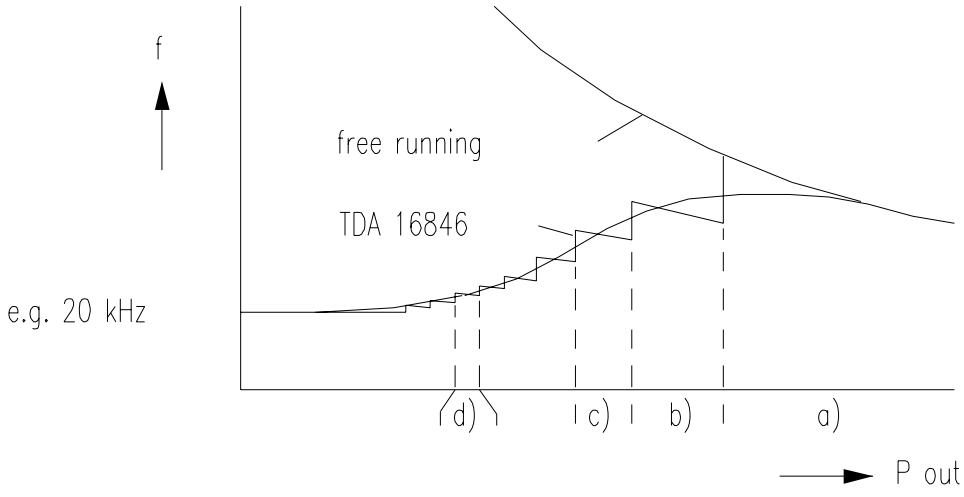

Fig. 2: Load dependent frequency course

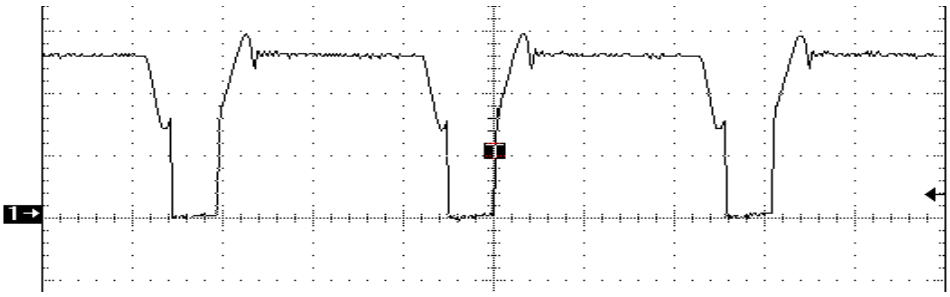

Fig. 1a: Drain voltage with switch on at the 1. zero crossing

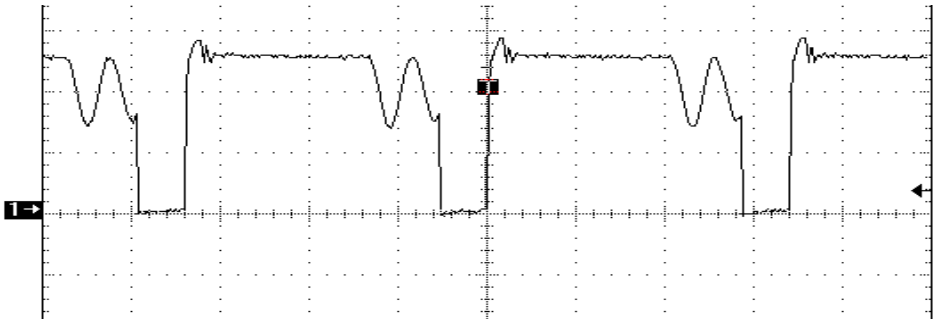

Fig. 1b: Drain voltage with switch on at the 2. zero crossing

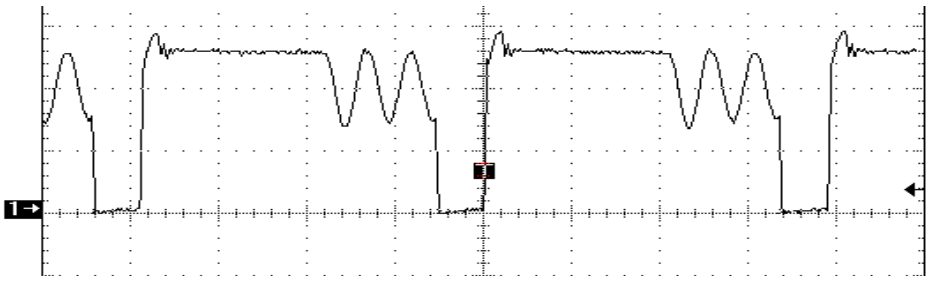

Fig. 1c: Drain voltage with switch on at the 3. zero crossing

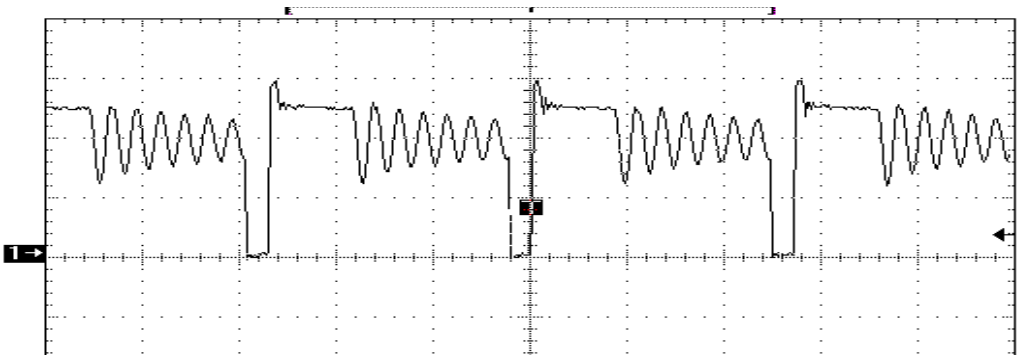

Fig. 1d: Drain voltage with switch on at the 7. zero crossing

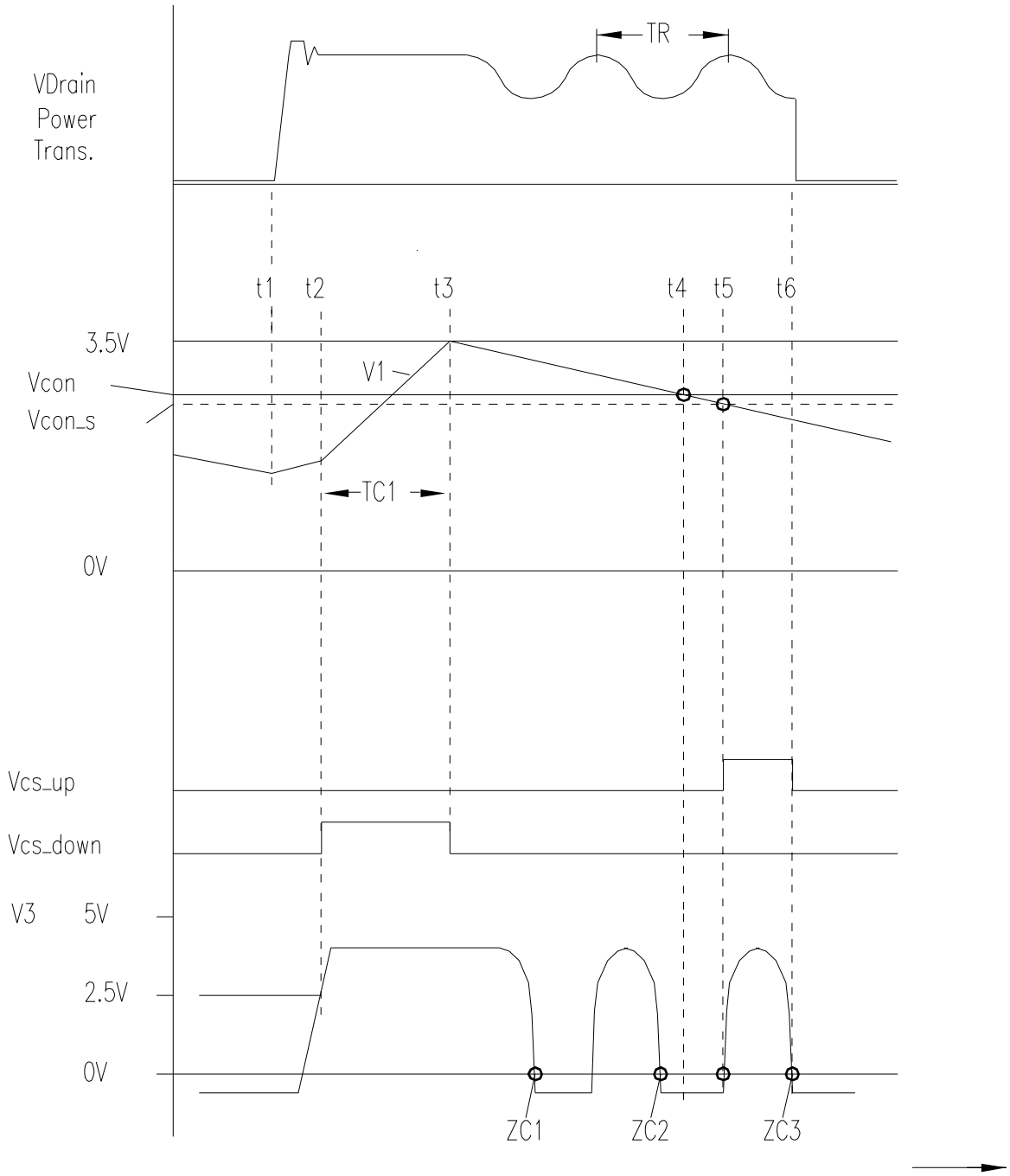

Fig. 3: Pulse Diagram of Off Time Circuit and Anti Jitter Circuit

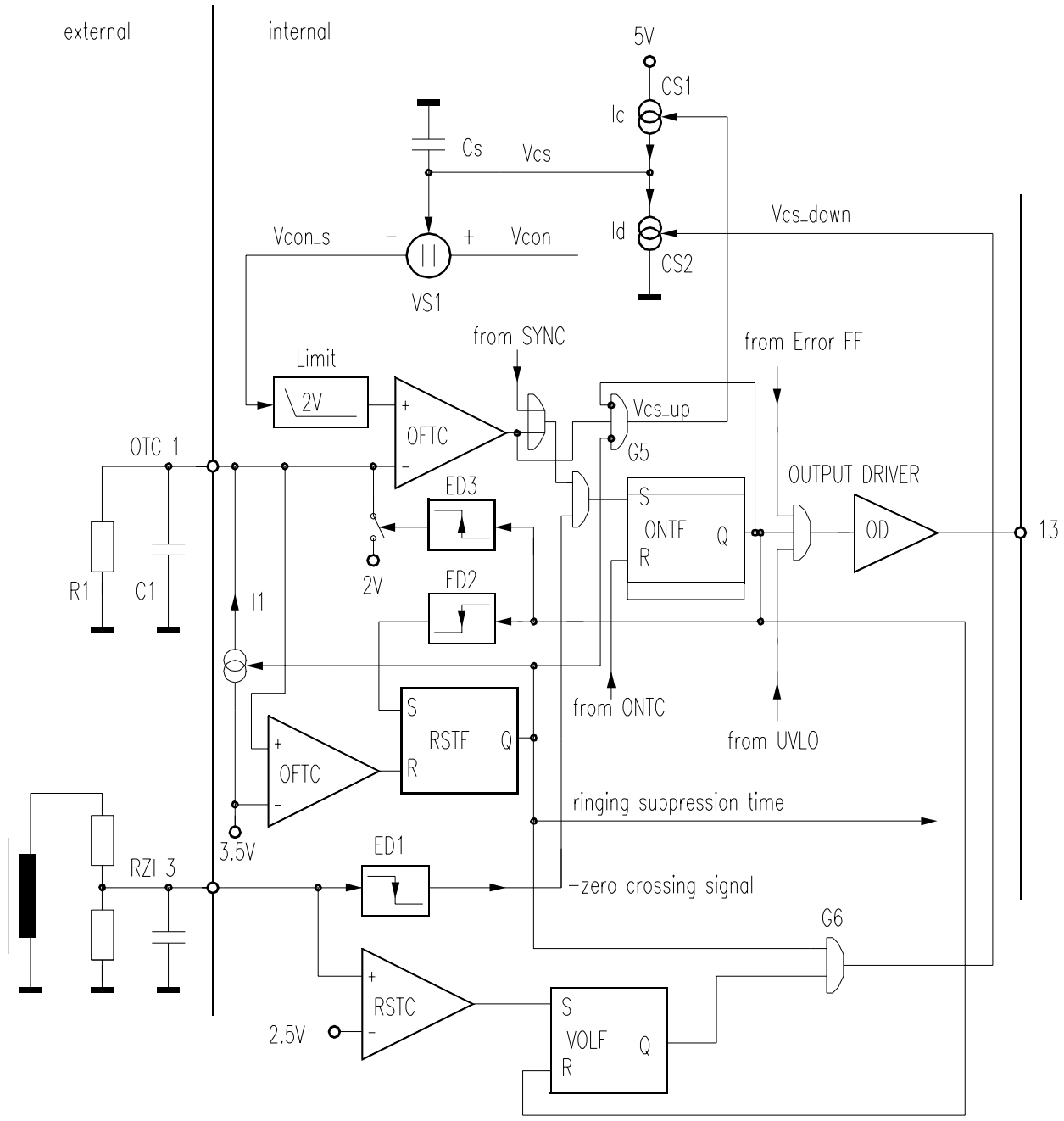

Fig. 4: Off Time Circuit with Anti Jitter Circuit

3. Function of the Power Factor Correction Circuit (PFC)

The mains input current of Switched Mode Power Supplies (SMPSs) with a capacitor input filter is not sinusoidal like the mains voltage but has a pulsed shape. The power factor correction circuit must make the mains input current more sinusoidal like the mains voltage. This is necessary to comply with the requirements of the new line-harmonics regulation EN 61000-3-2. The TDA 1684X is specialized for controlling the Charge Pump Circuit for PFC.

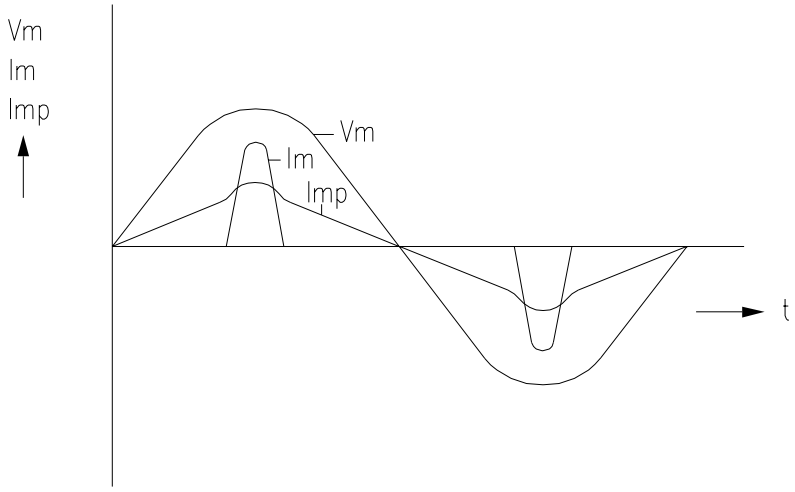

Fig. 5: Course of voltage and current
in the Standard and PFC Power Supply

In Fig. 5 can be seen that the input current Im of a standard power supply without PFC flows only during a short time near the pos. and neg. maximums of the mains voltage. No current is flowing outsides of the maximums. The reason is that the rectifier diode is only forward biased by the AC line voltage being higher than the voltage at the primary capacitor for a short time at the peak of the waveform.

To remedy this, a charge pump circuit is inserted between the bridge rectifier and the primary capacitor, which “pumps” current from a lower voltage up to a higher voltage to get a current shape like the curve Imp in Fig. 5. The current transfer of the charge pump is dependent on the load due to the frequency and pulse width modulation of the TDA16846, and by selection of the pasive L and C charge pump components.

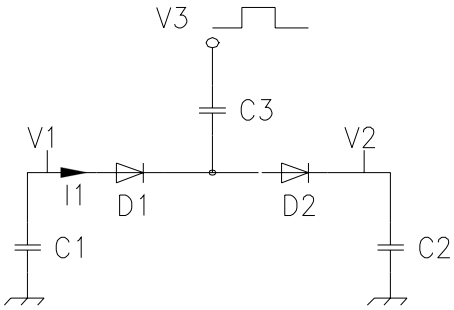

Fig. 6: Charge Pump Circuit

Fig. 6 shows a simple charge pump circuit. The capacitor C1 is charged with a DC voltage V1 and the capacitor C2 is charged with a DC voltage V2. V1 is a low voltage and V2 is a comparative high voltage. The charge pump circuit between V1 and V2 consists of the 2 diodes D1 and D2 and the capacitor C3. The capacitance of C3 is small compared with C1 and C2. Pulses from a voltage source V3 are transfered across the capacitor C3 to the connection point between D1 and D2. If the amplitude of the pulses V3 is higher than the difference V2 - V1, then a current flow is possible from voltage V1 up to the voltage V2. The charge Q3 which is transfered within each period across C3 is: Q3 = C3 * (V3 - (V2 - V1)) = C3 * (V3 + V1 - V2). When the pulse frequency is f3, then the current I1 of the charge pump is:

$$I1 = C3 \times f3 \times (V3 - V2 + V1)$$

If the voltage V1 is no DC voltage but a rectified AC voltage and if V3 = V2, then the current I1 becomes the same shape as V1.

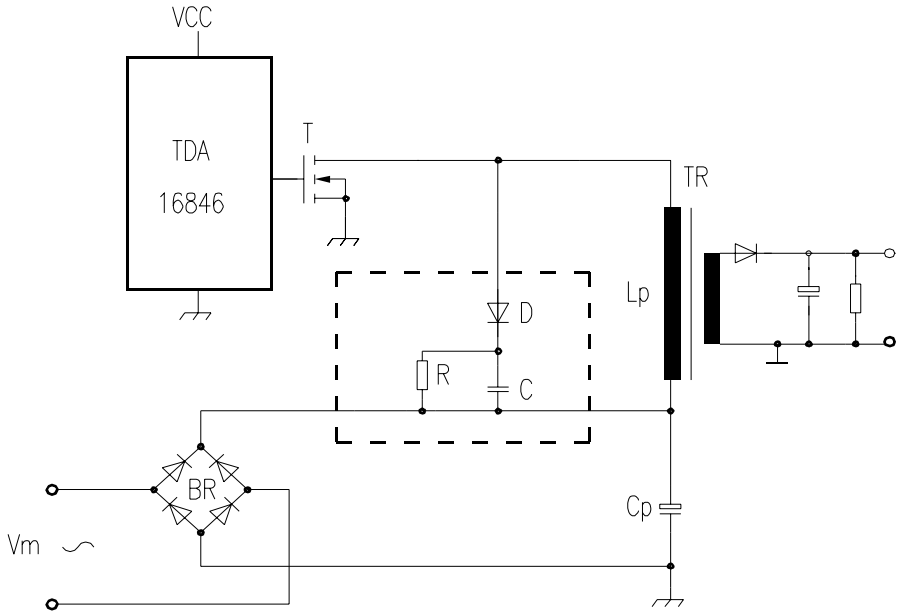

Fig. 7: RCD Snubber Circuit

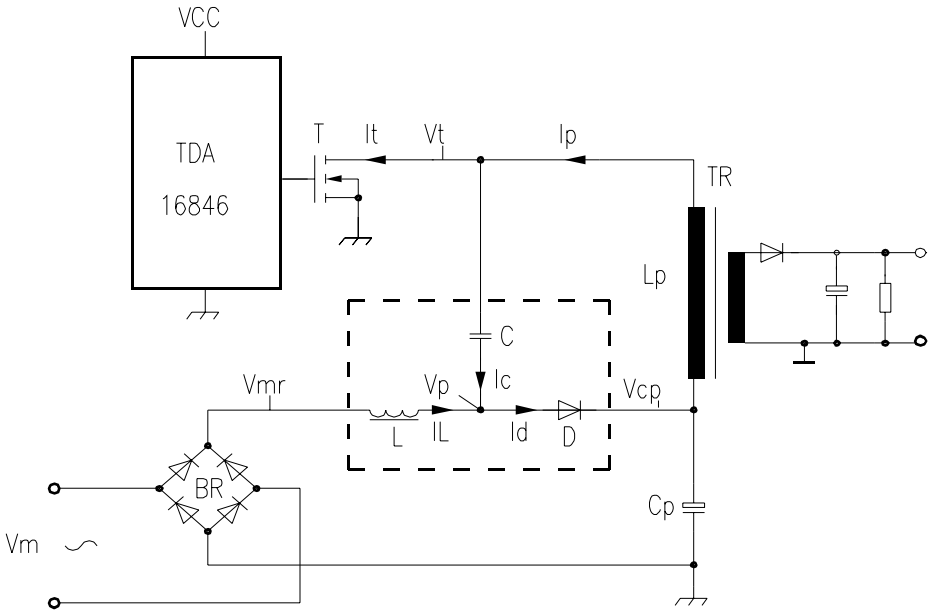

Fig. 8: PFC Charge Pump Circuit

In Fig. 7 a snubber circuit is shown which is generally used in standard SMPSs. It consists of a diode D, a resistor R, and a capacitor C. This snubber circuit cuts off the voltage overshoots at the drain of the switching transistor T. It can be replaced by a charge pump circuit consisting of an inductor L, a diode D and a capacitor C. Fig. 8 shows the charge pump circuit which is connected between the bridge rectifier BR, the positive terminal of the primary capacitor Cp and the drain of the switching transistor T. The bridge rectifier replaces the diode D1 in Fig. 6. The inductor L is put in to avoid high current pulses when the capacitor C charges after switching on the power transistor T. The pulsed voltage source V3 in Fig. 6 is replaced by the drain voltage of the switching transistor T. The snubber circuit shown in Fig. 7 is no longer necessary because the charge pump circuit fulfills not only the PFC- but also the snubber function.

Any transformer overshoots are intercepted by the charge pump, by forming a tuned circuit from the capacitor C and the transformer´s primary inductive resistance Lp, at the beginning of the transformer demagnetization period with a conducting diode D. This reduces the frequency and the amplitude of the overshoot to an acceptable level. This type of pulse snubbing has the advantage that no energy is lost, and this increases the efficiency level of the power supply.

The advantages of the PFC charge pump circuit are its simplicity, and the ease with which its transfer function can be controlled by dimensioning its components. A switched mode power supply can quickly be converted to PFC by selecting the appropriate configuration (as an alternative to the snubber circuit). Since the capacitor in the charge pump circuit is a differentiator, the charge transfer can be controlled effectively by means of the frequency. For example, the transfer function of the input current can be shaped by means of power supply phase dependent frequency modulation of the SNT frequency.

Next the function of the PFC charge pump circuit is explained in detail using the pulse diagram of Fig. 9. The voltage and current characteristics are depicted for a 230 V mains voltage. At the time t0 the switching transistor T is turned on by the control circuit TDA 1684X. The drain voltage Vt falls from about 600 V to 0 V. The primary current Ip begins to rise simultaneously due to the voltage imposed across the primary inductance. The voltage fall of Vt is also transfered accross the capacitor C to the junction between L and D (Fig. 8), so that the voltage Vp drops from 400 V to approx. -200 V. Due to the negative voltage Vp the current IL in the choke L is increasing. As this current charges the capacitor C the voltage Vp climbs likewise during t0 and t1.

After the charge phase of the flyback transformer TR and the choke L has been completed at time t1, the power transistor T is turned off by the control circuit TDA 1684X. The voltage Vt and with it the voltage Vp will rise rapidly until Vp has reached the potential Vcp (400V). The voltage Vp stays at the Vcp level while Vt slows its rise.

At the same time the current IL, which previouly charged the capacitor C, flows through the diode D into the capacitor Cp. The energy stored in L is then transferred to Cp. This causes a flow of current from the lower instantaneous value of the mains voltage to the higher voltage Vcp of the capacitor Cp.

Because of the conducting diode D an RC circuit is built of the primary inductance Lp and the capacitor C. The primary current is flowing through Lp, C and D until the moment t2, when the secondary diodes become conducting and the discharging of the transformer to the secondary side begins.

During the discharge phase from t2 to t3 the current IL is decreasing. The voltage Vp is clamped at one diode drop above Vcp.

The current through the choke L becomes higher with longer switch on time of the transistor T. The on time of T increases with an increasing secondary load and also with a decreasing mains voltage. At the same time the current increases through the PFC charge pump circuit.

Due to the stored energy in the capacitor Cp the power supply is also completely capable of stabilizing the power line ripple voltage during mains voltage´s zero crossing.

Fig. 9 shows also another period of the PFC charge pump circuit. This kind of sequence occurs near the maximum of the mains voltage. Vp is rising and reaches the potential Vcp during the switch on time from t3 to t5 at the time t4. So the current Ic stops at t4. The drain current It has 2 maxima. It consists between t3 and t4 of the sum of Ip and -Ic, after t4 only of Ip. In this kind of sequence the current IL doesn’t periodically return to zero.

There is no problem when the core of the PFC choke L gets nearly into saturation, because the current through L is limited by a charge of the capacitor C.

Attention: Because of the higher voltage at the primary capacitor which is necessary for the demagnetization of the PFC choke, a 450 V type instead of a 385 V type should be used.

To avoid that a current flows backwards through the PFC choke, the diodes for the bridge rectifier should be fast types, at least the two diodes at the output of the bridge rectifier should have a small reverse recovery time. Otherwise the function of the charge pump circuit can be heavy affected and the PFC diode can get an overvoltage.

The output voltages which are not regulated by the optocoupler can have a slightly higher mains voltage ripple because the PFC charge pump circuit effects an additionally modulation of the SMPS frequency with the mains frequency. This effect is higher with a weak coupled transformer.

A complete circuit diagram of a SMPS with the PFC charge pump circuit can be seen in Fig. 16. The PFC charge pump circuit consists of the components L08, D08, and C08.

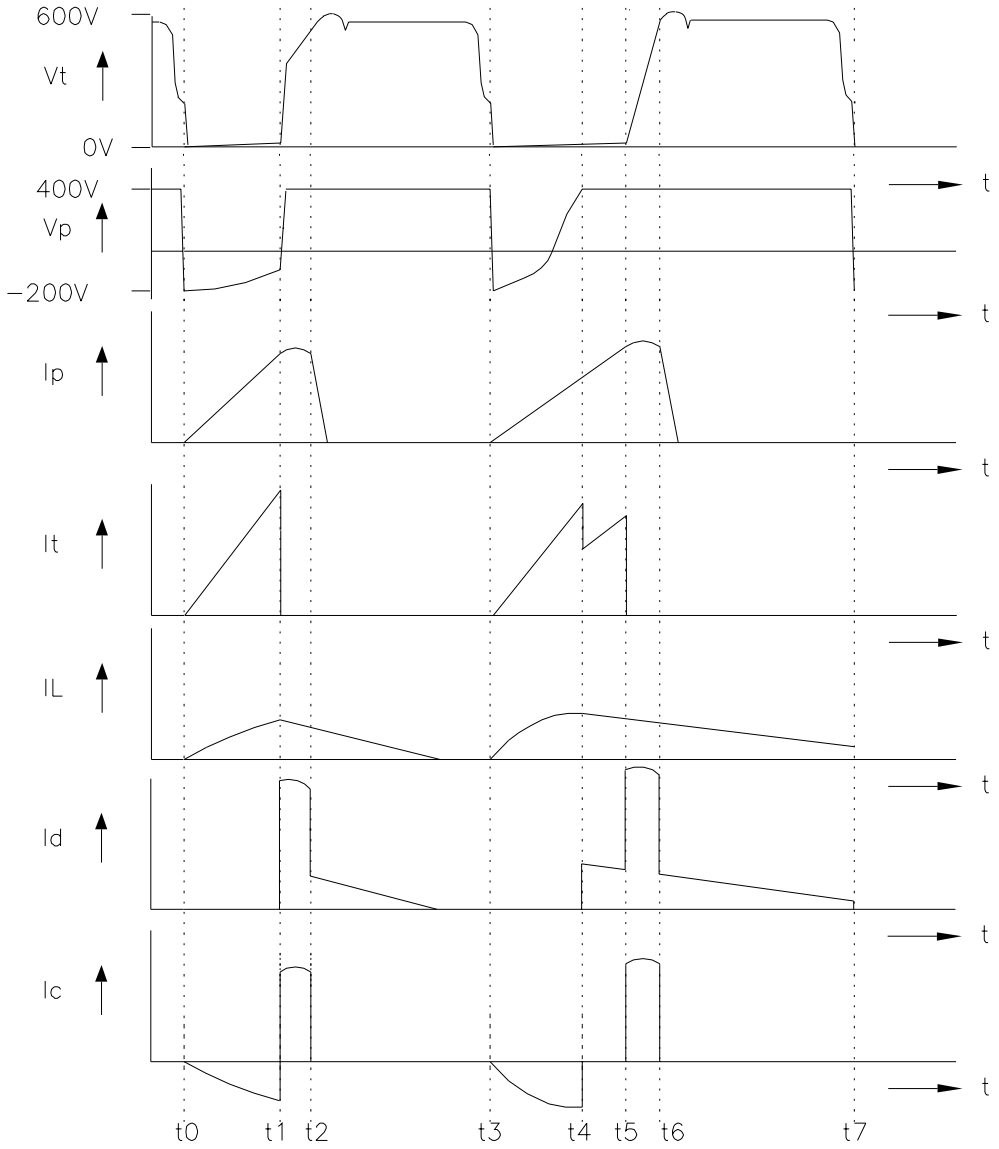

Fig. 9: Voltages and currents in the PFC Charge Pump Circuit

4. Function of the Control Circuit

Fig. 10 shows the internal control circuit of the TDA 1684X. The control voltage is stored in the external capacitor at pin 4. This capacitor is charged periodically by the current cource CS3 and is discharged by the current source CS4. The pulse for charging is produced by the output of gate G6. The inputs of G6 are the output of the ringing suppression time flipflop RSTF and the output of the ringing suppression time comparator RSTC. The pulse for discharging comes from the error amplifier EA. The timing for charging and discharging can be seen in the pulse diagram Fig. 11. The charging pulse V4_up begings at the time t1, when the pulses at pin 3 V3 exceed the threshold 2.5V, and ends at the time t4, when the voltage V1 at pin 1 reaches 3.5V (end of ringing suppression time). Discharging occurs during the time when the pulses at pin 3 exceed the 5V reference voltage between t2 and t3. During running regulation parts of the pulses at pin 3 exceed the 5V reference voltage, so that at constant load the charging current is equal to the discharging current on an average and the voltage at pin 4 is constant. When the load becomes higher, then the voltage at pin 4 becomes higher and vice versa.

When the buffered control voltage Vcon becomes lower than 2V, the amplitudes of the charging and the discharging pulses are reduced. The occurs because at light loads the gain of the regulation becomes higher because of the very small switch on times. To avoid the danger of regulation oscillation, the charging and the discharging currents are reduced gradually within the control voltage range 2V to 1.5V by a factor of 4 as shown in the diagram Fig. 12. In the control voltage range 2V to 5V the amplitude of the charging pulses is 700 µA and that of the discharging pulses 1400 µA. When the control voltage goes down from 2V to 1.5V, the charging current is reduced to 170 µA and the discharge current to 340 µA. This is done by a Control Voltage Converter CVC and a Control Voltage Inverter CVI (Fig. 10). The output of CVI regulates the amplitude of the current sources CS3 and CS4.

If an opto coupler is used, its output should be connected between pin 5 (OCI) and ground. Between pin 5 and the reference voltage 5V an internal pullup resistor R1 (20 kOhm) is integrated on the chip. To put the primary regulation out of operation, the external voltage divider at pin 3 should be changed in this way so that the pulses at pin 3 are higher than 2.5V but lower than 5V. Pin 3 then only acts as zero crossing input and as additional overvoltage protector, when the opto coupler circuit drops out. As always the lower of both signals at the positive input of the Buffer for Control Voltage BCV becomes operative, the voltage at pin 5 which is now lower than the voltage at pin 4 is used for the control. The error amplifier of the external opto coupler circuit is active and the internal error amplifier EA is inoperative.

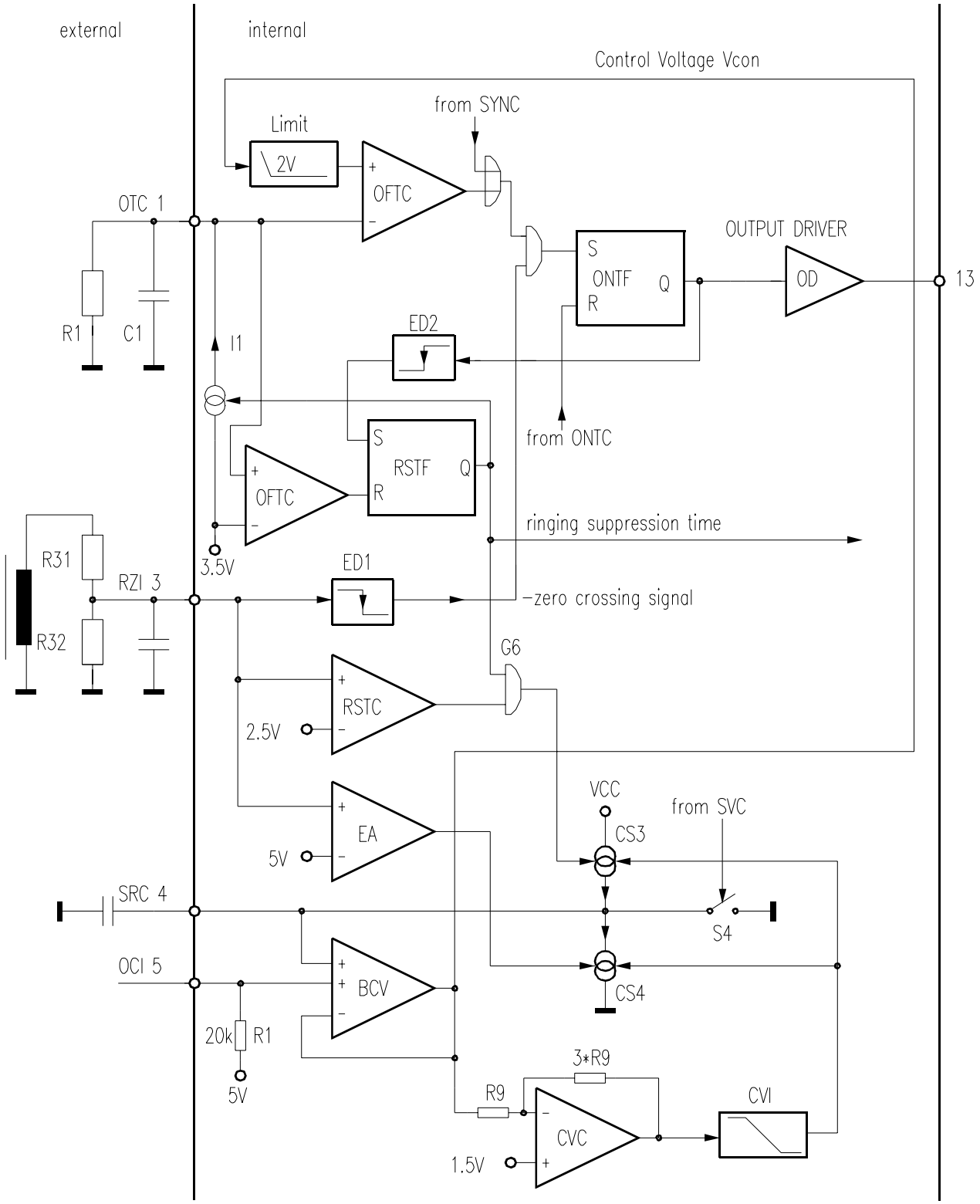

Fig. 10: Control Circuit

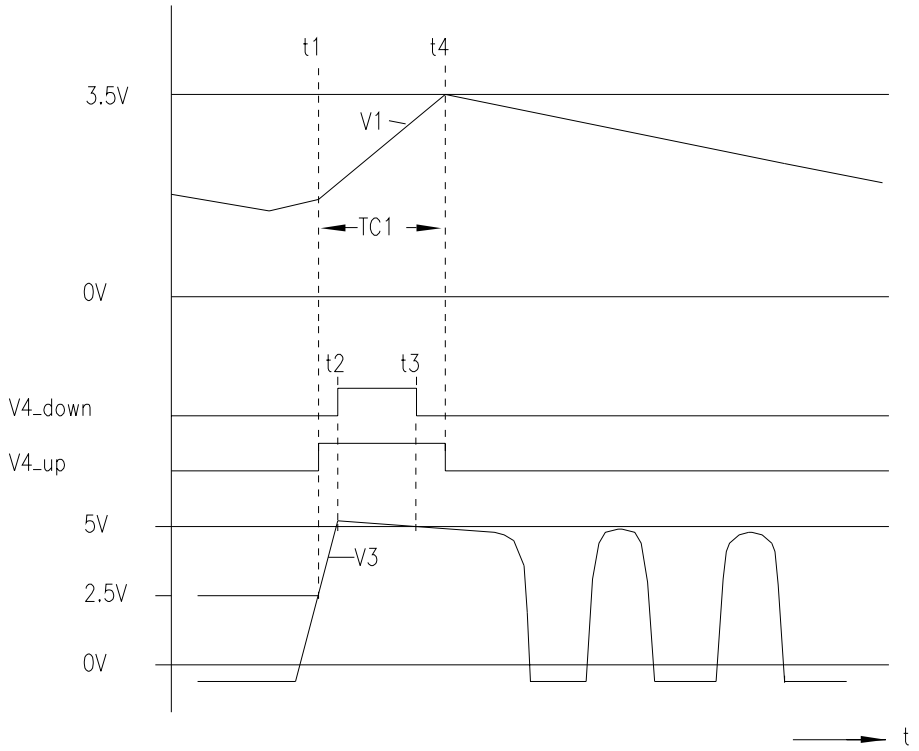

Fig. 11: Pulse Diagram of Control Circuit

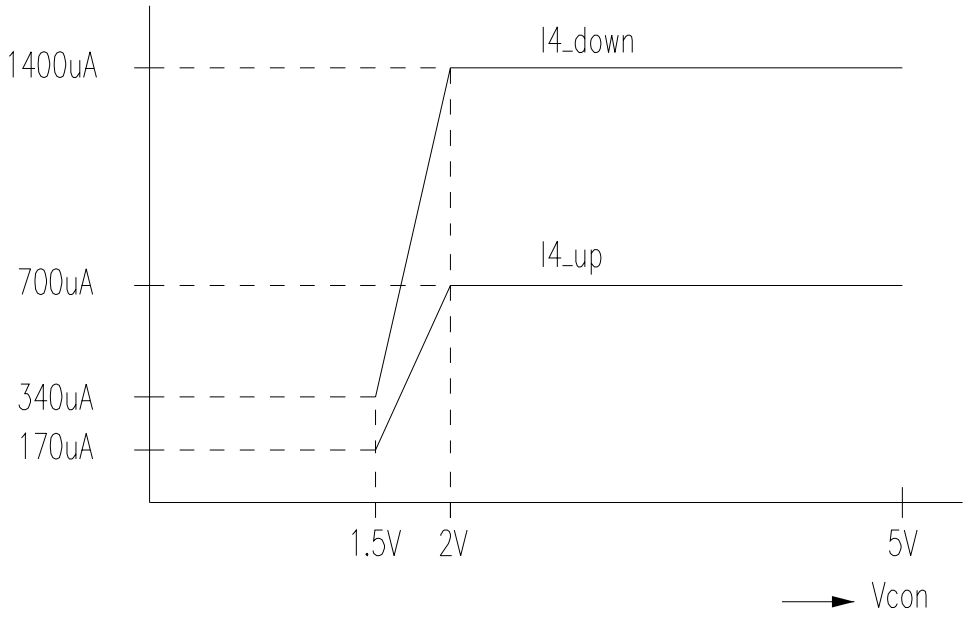

Fig. 12: Pin 4 Charge and Discharge Current

5. Function of the Fold Back Point Correction

The fold back point correction is necessary in free running SMPSs to make the maximum possible output power largely independent of the mains voltage. Without this function the maximum possible power would increase with higher mains voltage. First some of the relationships are shown with mathematically.

Following symbols are used:

Et:	Stored magnetic energy in the transformer
Ip:	Peak current through the primary winding
Lp:	Inductivity of the primary winding
np:	Number of turns of primary winding
ns:	Number of turns of secondary winding
P:	Specified max. power
R2 * C2:	RC circuit at pin2
R23:	Resistor between pin 11 and pos. terminal of primary capacitor
R24:	Resistor between pin 11 and ground
toff:	Switch off time (= demagnetization time)
ton:	Switch on time
V2:	Peak voltage at pin 2 of TDA 1684X at constant power P in dependence of Vp
V2max:	Max. allowed peak voltage at pin 2
Vp:	DC voltage at primary capacitor (rectified mains voltage)
Vs:	DC voltage at secondary output

The calculation is based on the following formulas:

1)

$$Et = \frac{1}{2} \times Vp \times Ip \times ton$$

2)

$$\frac{Vp}{np} \times ton = \frac{Vs}{ns} \times toff$$

3)

$$Ip = \frac{Vp \times ton}{Lp}$$

4)

$$C2 = \frac{Vp \times ton}{R2 \times (V2 - (1,5V))}$$

5)

$$P = \frac{Et}{ton + toff}$$

Substituting Equation 1), 2), 3) and 4) into equation 5) results in equation 6) when Vt is defined as:
Vt = Vs * np / ns

6)

$$V2 = \frac{2 \times Lp \times P \times \left(1 + \frac{Vp}{Vt}\right)}{Vp \times R2 \times C2} + 1,5V$$

In Fig. 14 the circuit diagram of the fold back point correction is shown. The max. output power is reduced at high mains voltage by reducing the max. control voltage depending on the voltage at pin 11, the input of the primary voltage check. When V11 exceeds 1.5V, then the output of the Primary Voltage Amplifier PVA becomes lower than 1.5V. So the voltage at pin 5 which is originally 5V is reduced across the diode D5 and a voltage source of 3.5V. As the gain of PVA is 1/3, determined by the resistors R6 and R6 * 1/3, the correlation between Vp and V2max is:

7)

$$V2max = 5V - \frac{Vp \times \frac{R24}{R23 + R24} - (1,5V)}{3}$$

The correlations between V2 resp. V2max and Vp are drawn in the diagram Fig. 13. As an example a 100 W wide range SMPS has been taken for the calculations with the dimension:

P = 100 W, R2 = 1 MOhm, R23 = 3.9 MOhm, R24 = 47 kOhm, C2 = 470 pF, Vs = 80 V. Transformer: AL = 190 nH, Ae = 125 mm², Lp = 475 µH, np = 50, ns = 37.

V2 is the peak voltage at pin 2 which is equal to the control voltage Vcon in dependence of the rectified mains voltage Vp at constant power P. V2max is the allowed peak voltage according to the fold back point correction circuit. Fig. 13 shows that at min. and max. mains voltage V2max is nearly equal to V2. The difference between V2max and V2 in the middle of the mains voltage range means an increasement of the max. power of about 10%, because (V2-1.5V) ~ P (s. Eq. 6)). Without fold back point correction the increasement of the max. power would be about 30% at highest mains voltage against lowest mains voltage.

In fixed frequency and synchronization mode the fold back point correction is not necessary and is therefore switched off automatically by the TDA 1684X.

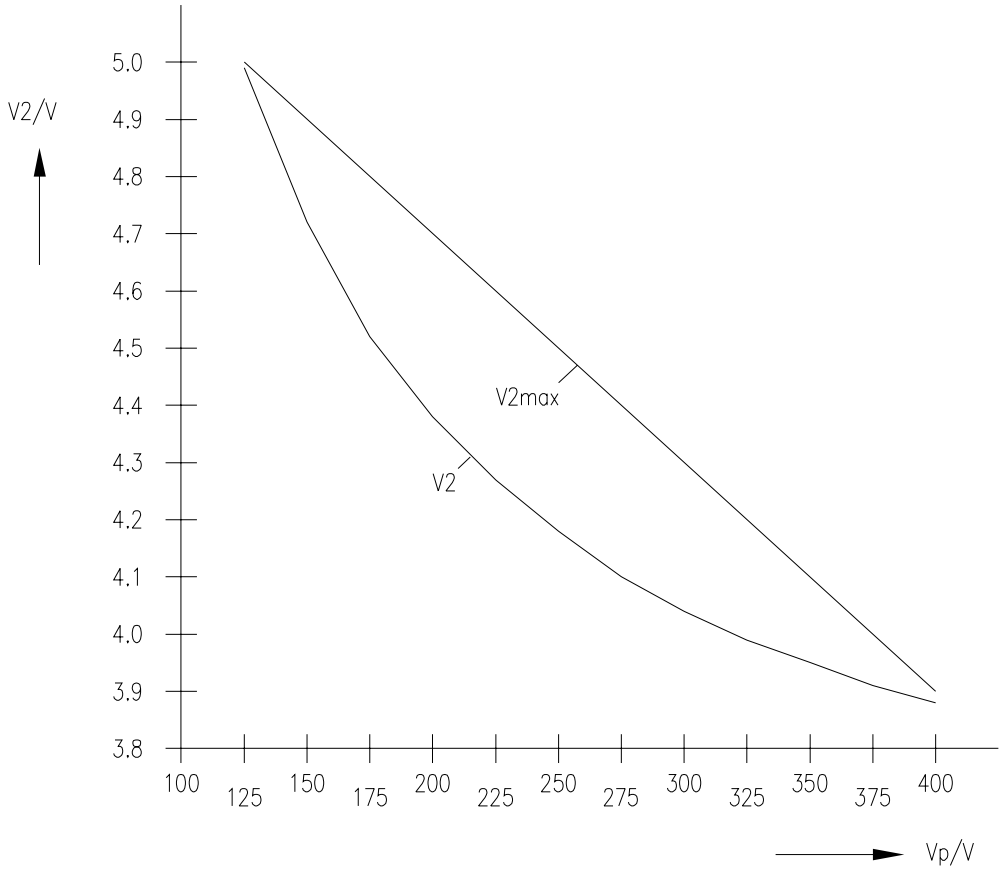

Fig. 13: Diagram Fold Back Point Correction

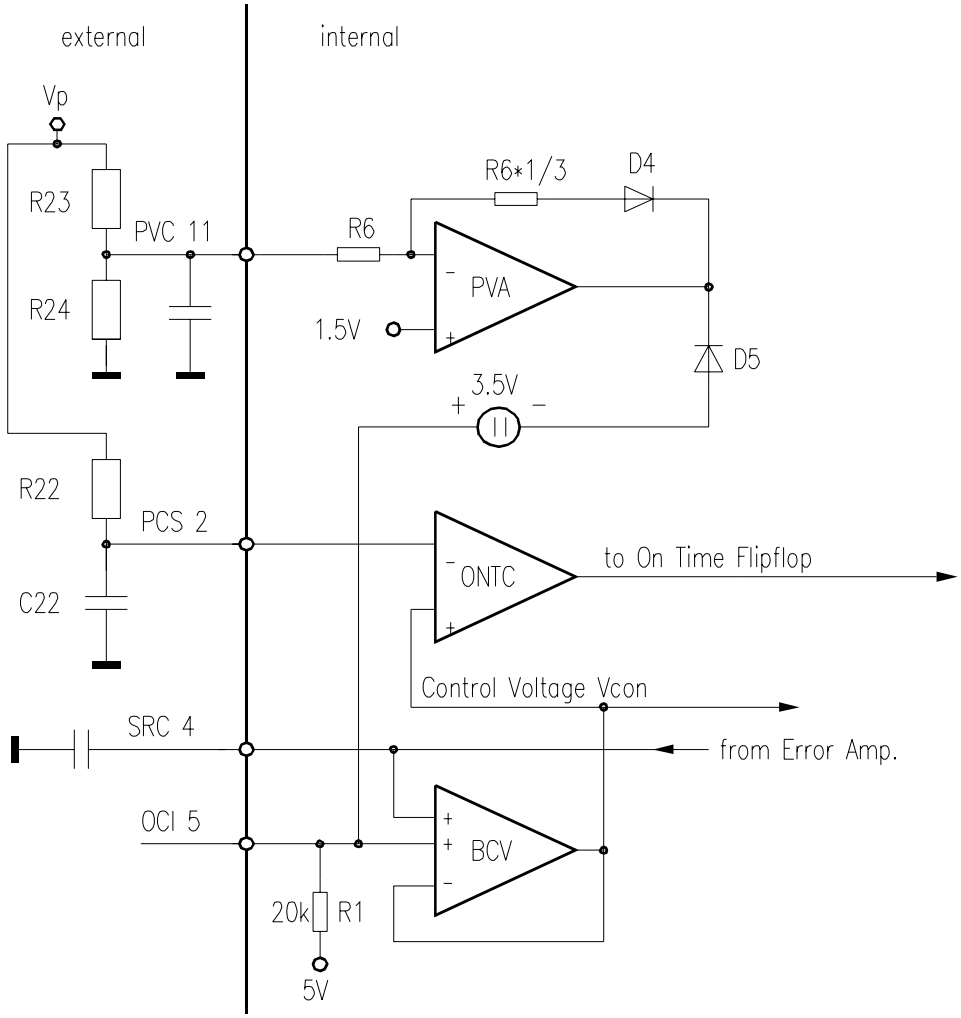

Fig. 14: Fold Back Point Correction

6. Modifications of the Load Dependent Frequency Path

The load dependent frequency path which is shown in Fig. 2 can be modified by additional external components. Therewith also the hysteresis of the anti jitter circuit can be magnified. This is advantagious in applications with periodically wobbling load e.g. in TVs. With the following method the load dependent frequency path can be altered in a wide range for each case of application.

The SMPS frequency is determined by the control voltage and the control voltage in turn is dependent on the shape of the rising voltage of the primary current simulation at pin 2. Normally the voltage at pin 2 starts at 1.5 V and rises maximal up to 5 V. This is shown in Fig. 15 with curve V2ori. Onother curve V2mod shows a modified voltage shape of V2 which can be achieved with a changed circuit at pin 2 (resistor in series to the capacitor and bigger capacitor) and an additional resistor between pin 5 and ground. At ton = 0 V2mod jumps first from 1.5 V up to 2.5 V. Starting from 2.5 V the voltage is rising up to max. 4V instead of 5V. So the starting point is lifted by 1V and the end point is lowered by 1 V. The control voltage range is narrowed from 3.5 V to 1.5 V. So also the contol voltage dependent lowering of the frequency is changed.

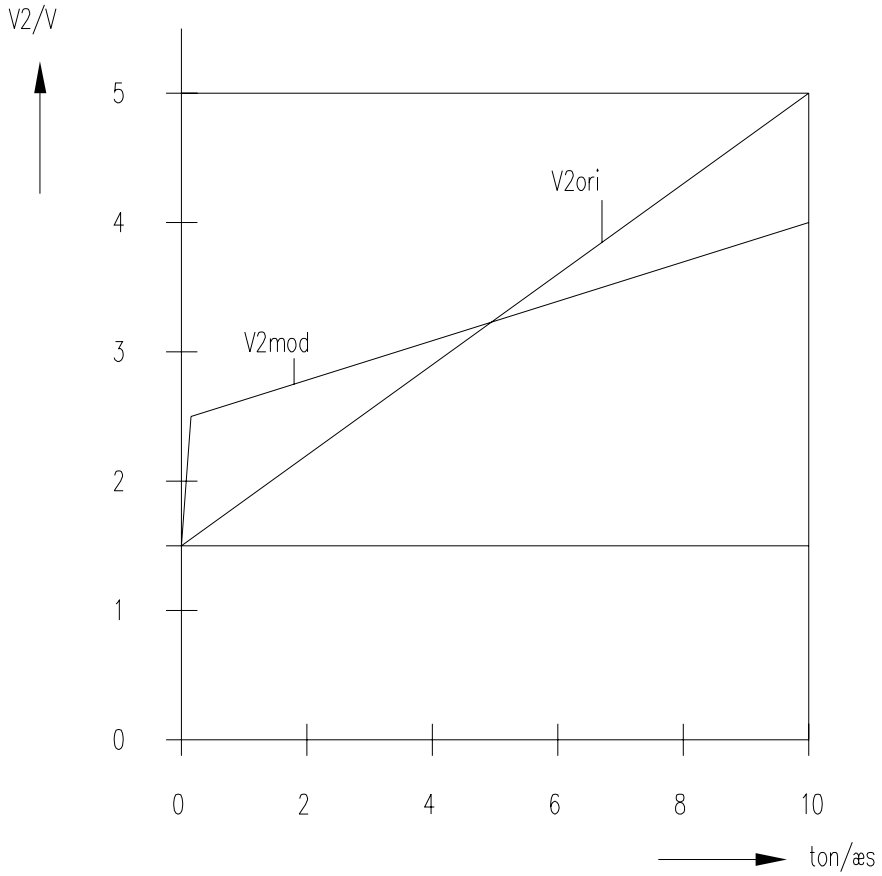

Fig. 15: Modification of V2 Voltage Rise

Shifting of the frequency path is also possible by connecting an additional resistor between pin 1 (Off Time Circuit) and the external RC circuit at pin 1. This resistor causes a voltage drop during charging of the capacitor at pin 1 by the internal current source of pin 1. The voltage of pin 1 is lowered after the charging time by this voltage drop and thus the point of intersection between the voltage at pin 1 and the regulation voltage V5 is shifted to the left. So switch on is possible already at the first zero crossing signal within a wide load range. The ringing suppression time and the standby frequency have to be new adjusted after this modification. This function can be seen in the pulse diagram Fig. 15a. A use of this method can be seen in the circuit diagram of the 200 W demoboard in Fig. 34.

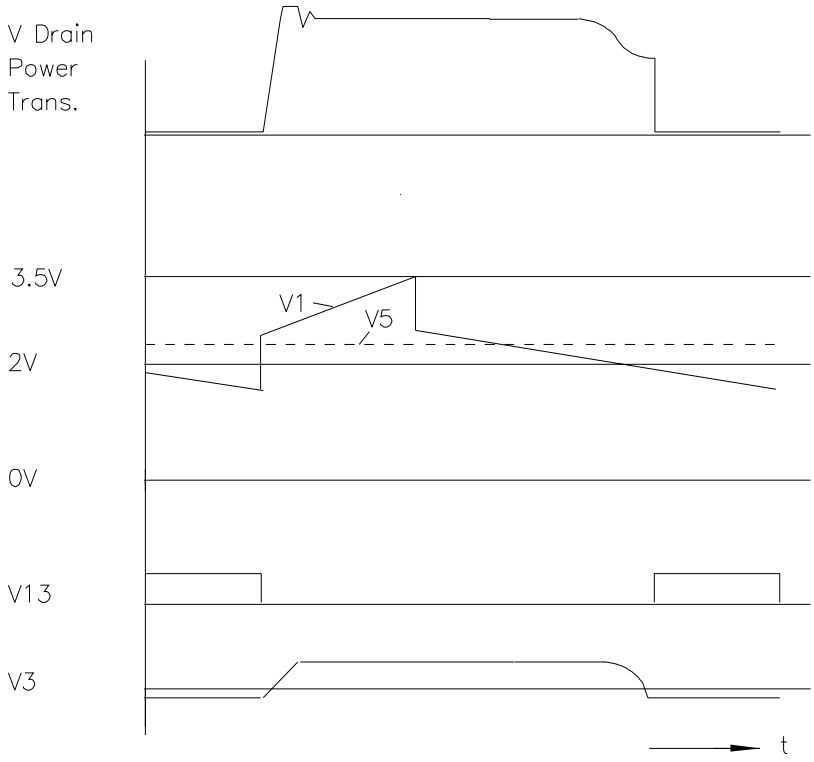

Fig. 15a: Pulse Diagram of the Modified Off Time Circuit

With both methods as described above (additional resistor at pin 2 and additional resistor at pin 1) a very big change of the frequency path is possible.

In the following figures some modified circuit diagrams for shifting the frequency path are shown. First Fig. 16 shows the original circuit of an application for TV with the PFC charge pump circuit. The max. input power is 100 W. When decreasing the output power the first frequency jump (switch on at the second zero crossing) occurs at 80 W input power. The standby frequency is 20 kHz.

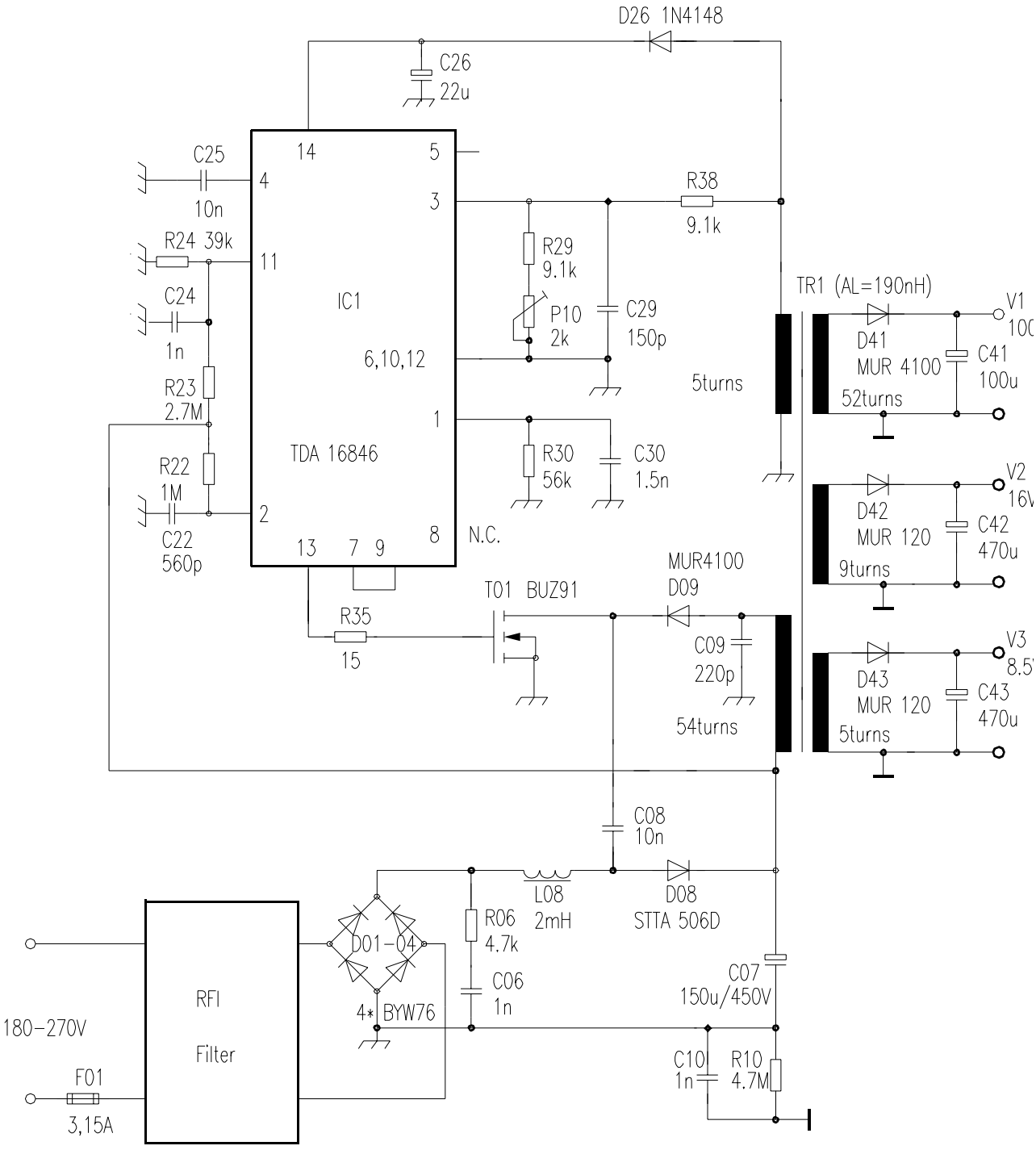

Fig. 16: Power Supply with TDA 16846 and PFC

Fig. 17 shows a modified circuit with shifted frequency path. A resistor R25 of 1.8 kOhm is put in between the capacitor C22 at pin 2 and ground. This resistor causes the voltage change of V2 at the begining of the switch on time. The reduction of the max. control voltage from 5 V to about 4 V is made by the resistor R28 (82 kOhm) between pin 5 and ground. A voltage divider is built with the integrated 20 kOhm resistor between pin 5 and 5 V internal reference voltage. The resistor R25 has also the effect of a fold back point correction because the voltage jump of V2 becomes higher with higher mains voltage, and so the control voltage range becomes smaller with higher mains voltage. The function of the internal fold back point correction is disabled by the diode D24. Because the voltage V2 is set to 1.5 V outside of the switch on time, the voltage V11 at pin 11 is limited by 1.5 V + Vbe. Because of the reduced control voltage range the capacitor C22 at pin 2 is enlarged from 560 pF to 1 nF. The maximum input power is now 108 W and the first zero crossing jump occurs at 74 W. The standby frequency remains unchanged.

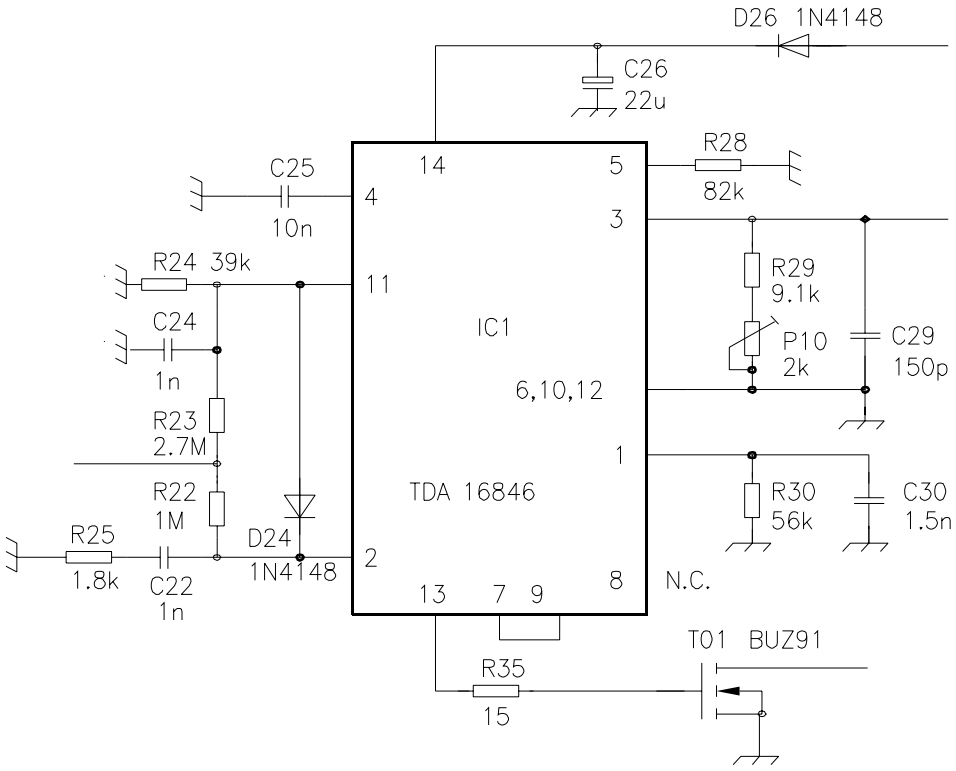

Fig. 17: Modified Pin 2 Circuit with 1 Resistor

In Fig. 18 the V2 voltage jump is made higher by the resistor R25 and the diode D22. The diode causes a nearly mains voltage independent voltage jump. The resistor R25 has to discharge the capacitor C22 after the switch on time. The resistor R26 causes a mains dependent part of voltage drop and fulfils the function of the fold back point correction. This SMPS has a maximum input power of 90 W and the first frequency jump occurs at 60 W. The standby frequency is raised to 25 kHz.

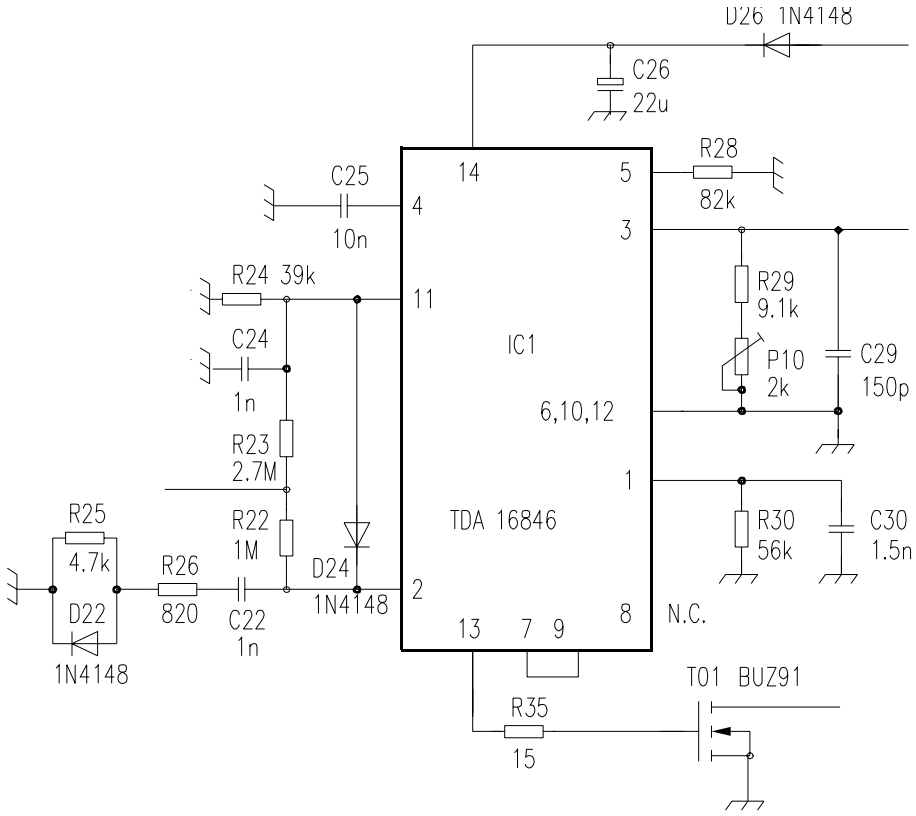

Fig. 18: Modified Pin 2 Circuit with 2 Resistors and 1 Diode

Fig. 19 shows a circuit with 2 diodes D22 / D23 between pin 2 and ground. The voltage jump of V2 is about 1.5 V. The resistor R25 is increased to 10 kOhm. Because the voltage drop across D22 and D23 is not exactly constant but depends on the current through the diodes, this effect is used for the fold back point correction. The diode D24 disables the internal fold back point correction. The capacitor C22 is 1 nF and the resistor R22 is reduced to 820 kOhm. The max. control voltage is not reduced (no resistor at pin 5). Because of the smaller control voltage range the control voltage capacitor C25 at pin 4 is raised to 18 nF. The max. input power amounts 100 W. During a wide power range the power transistor is switched on at the first zero crossing signal. The frequency reduction doesn't begin as early as at 36 W input power. The standby frequency is 30 kHz with R 30 = 68 kOhm.

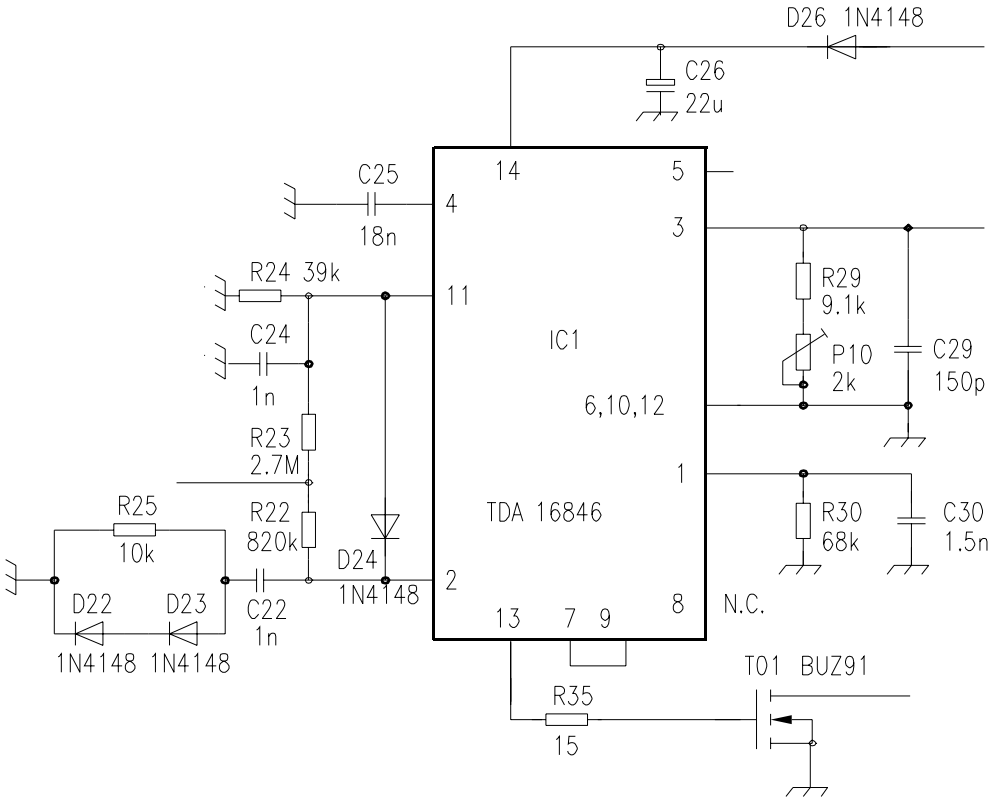

Fig. 19: Modified Pin 2 Circuit with 1 Resistor and 2 Diodes

7. Modifications of the PFC-, Mains Filter- and Snubber- Circuit

In Fig. 16 the PFC charge pump circuit consists of the components L08, D08 and C08. Additionally a diode D09 is built in between drain of T01 and the primary winding of the transformer pin 3. The diode D09 prevents a current flowing backwards through L08, C08 and the primary winding after discharging of the transformer. So this diode suppresses low frequency oscillations in free running mode with reduced frequency. Also the voltage at the primary capacitor C07 in standby mode is lowered. The low frequency oscillations would cause irregular SMPS periods and noise in the transformer.

The RC circuit R06 / C06 is a damping circuit and lowers the amplitude of pulses which occur near the zero crossing of the mains voltage between the output of the bridge rectifier and the PFC inductivity L08.

In PFC power supplies the mains filter circuit has to be made a little more expensive because additional RF- noise is transferred by the PFC capacitor C08. Especially the X- capacitors have to be made bigger. A reducing of the X- capacitors is possible by the mains filter circuit shown in Fig. 20.

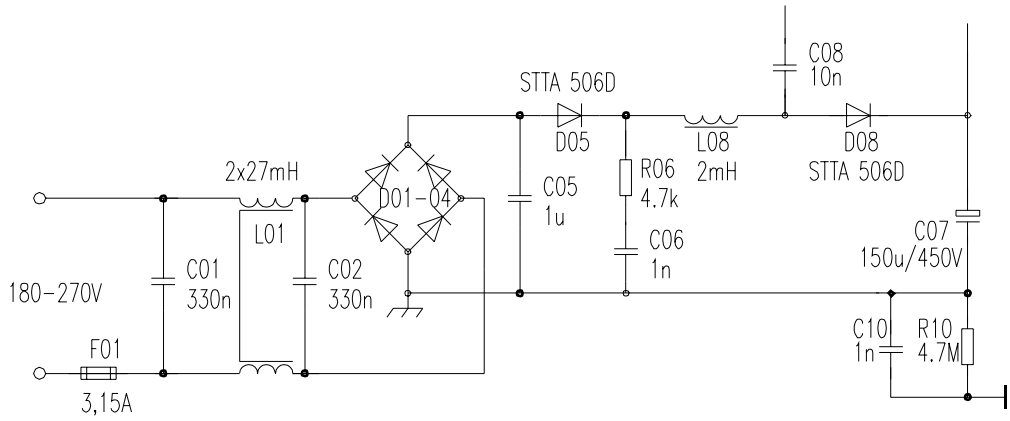

Fig. 20: Modified Mains Filter Circuit

Between the bridge rectifier D01-D04 and the PFC choke L08 an additional diode D05 is put in. Now a part of the X- capacitance can be transferred to the output of the bridge rectifier into the filter capacitor C05 (e.g. 1 µF). The bridge rectifier D01-D04 can consist of slower diodes but the diode D05 has to be a fast one. The additional advantage of this circuit is a lower idle current at the mains input because of the smaller X- capacitors.

In power supplies without PFC a snubber circuit has to be used which can be seen in Fig. 21. Transformer overshoots are intercepted by the snubber diode D10 and the snubber capacitor C11. C11 is discharged by a DC- current which flows through the resistor R11 and the Zener diode D11. The power dissipation of the snubber circuit depends on the cut off level of the overshoots. This is expecially important for standby mode. The amplitude of the overshoots is higher with higher output power. If no Zener diode D11 is used, the cutoff level has to be adjusted at max. output power and is then lower in standby mode which results in noticeably more power dissipation in standby mode. D11 has the advantage that the cutoff level can be essentially made indepedent of the output power and so set higher in standby mode. The resistor R11 is useful to protect the Zener diode D11.

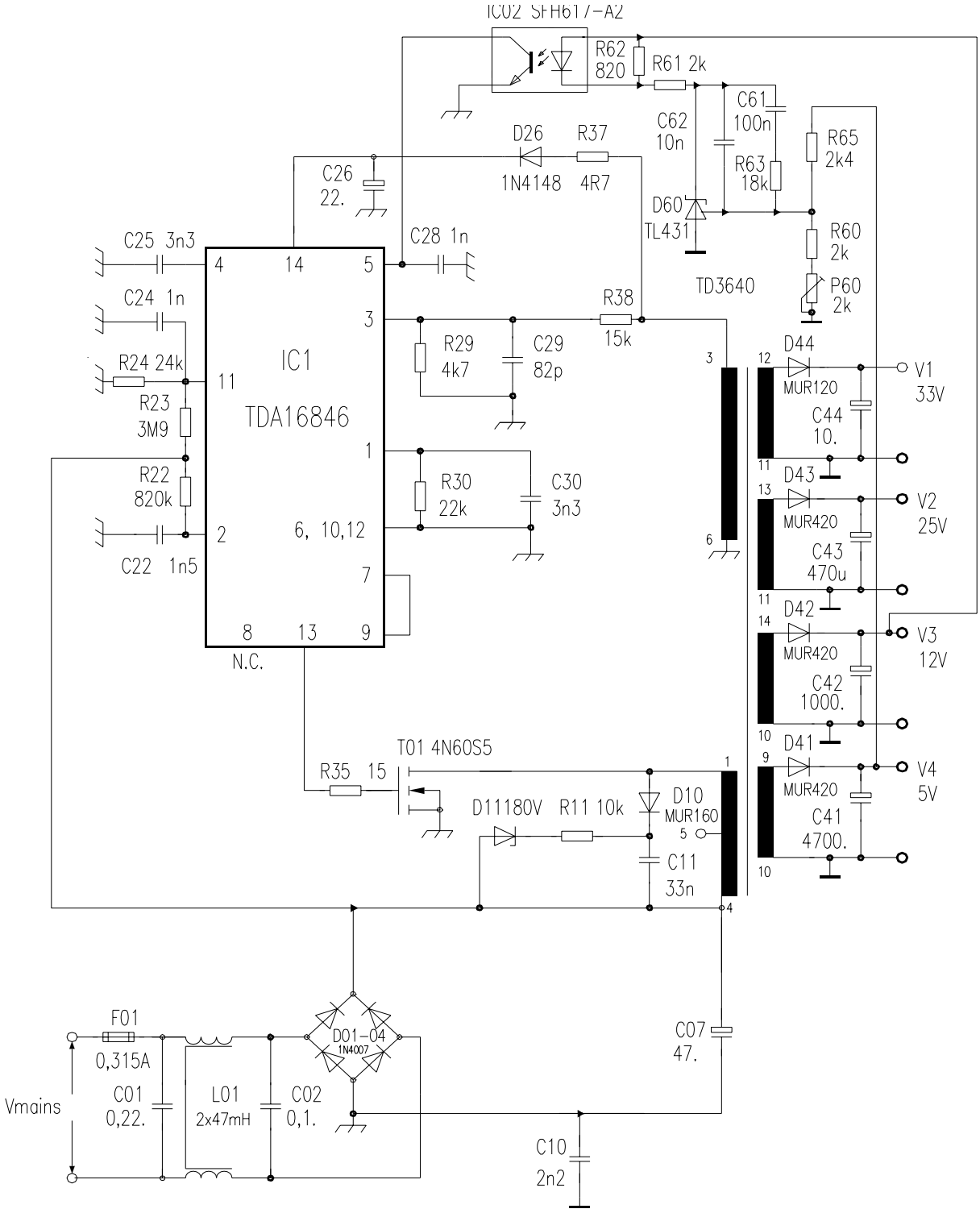

Fig. 21: Snubber Circuit with Resistor and Zener Diode

8. Applications for Freerunning Mode

SMPS Application for TV- Portable (60- 80 W, TD 3624)

Figure 22 shows a circuit diagram for a low range TV set without PFC but with opto coupler. For the MOS FET a Cool MOS transistor 4N60S5 is used. The snubber circuit consists of a simple RCD circuit (R11, C11, D10). A serial resistor R37 (20 Ohm) lowers the pin 14 supply voltage. To heighten the hysteresis of the internal anti jitter circuit, the control voltage range is lowered by the resistor R31 (82 kOhm) between pin 5 and ground as explained in chapter 6. The Zener diode D61 (Z3.3V) stabilizes the secondary voltage V4 in standby mode when only this voltage is charged. Therefore the voltage V1 rises above its normal value of 135 V in standby mode. The control behaviour is determined by the fold back circuit R63 / C61 at the reference circuit D60 (TL 431). The capacitor C62 suppresses noise at high mains voltage.

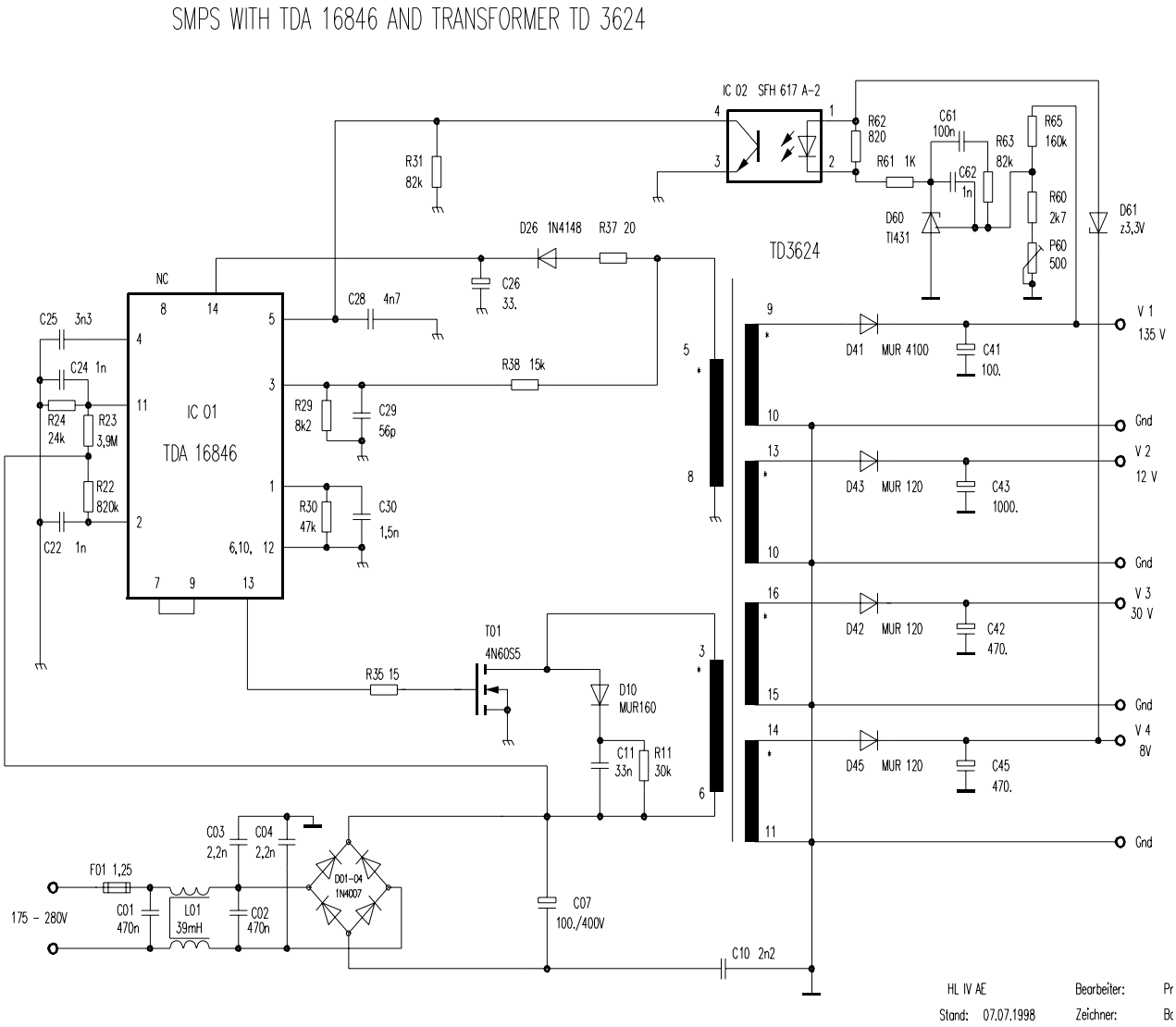

Fig. 22: SMPS for TV Portable

SMPS Application for TV- Mid Range (100 - 120 W, TD 3612)

In the SMPS shown in Fig. 23 the PFC charge pump circuit is built in (L08, D08, C08, D09) and the modified mains filter circuit as explained in chapter 7 (C05, D05). For standby mode, the output voltage V4 is stabilized by the Zener diode D61 (Z4.3V). For lowering the voltage V3 in standby mode this voltage is charged with the resistor R42 (5.6 kOhm). The high output voltage can be switched between 110 V (V1) and 105 V (V2). After switching between V1 and V2 the actual voltage has to be adjusted with poti P60 (500 Ohm). As in SMPS TD 3624 the V14 supply voltage is lowered with resistor R37 (6.8 Ohm) and the max. control voltage is lowered with resistor R36 (47 kOhm) as explained in chapter 6.

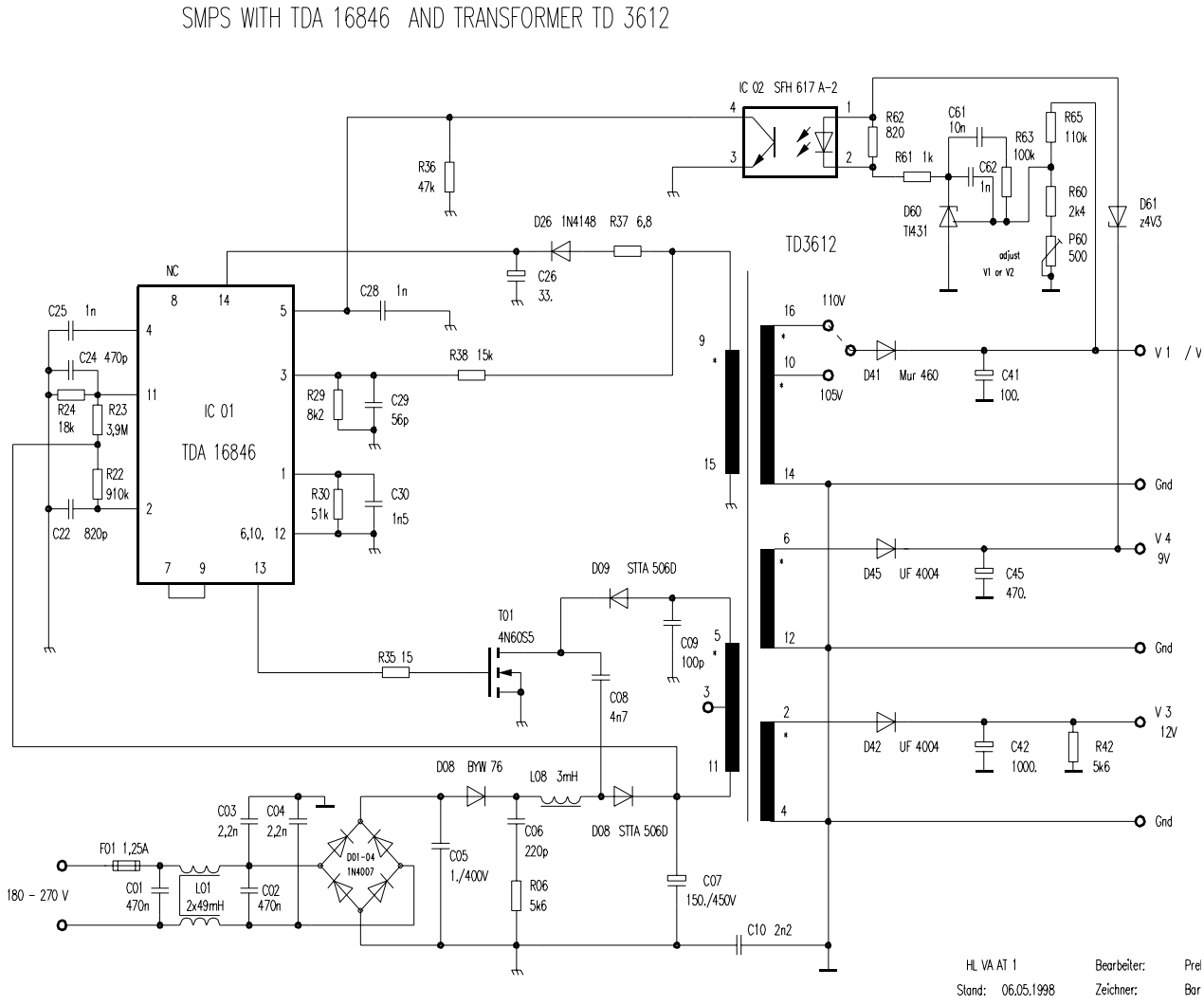

Fig. 23: SMPS for TV Middle Range

SMPS Application for TV- High End (200 W)

Fig. 24 shows a SMPS for a High End TV Set with 200 W power and mains voltage wide range (90-270 V). To reduce power dissipation in the MOS FET T01 the gate resistor is only 3.3 Ohm. To get a very fast switch off, a diode D36 (1N4148) is connected parallel to R35. All power components are dimensioned robustly according to the high output power. Many of the diodes at the primary and the secondary side are provided with heat sinks. For the transformer core the type E55/28/21 with an air gap of 3 mm has been chosen. With higher air gap more energy can be stored in the transformer with lower magnetization. Also the cross sections of the wires in the windings are adapted to the high currents. Partial windings are connected in parallel.

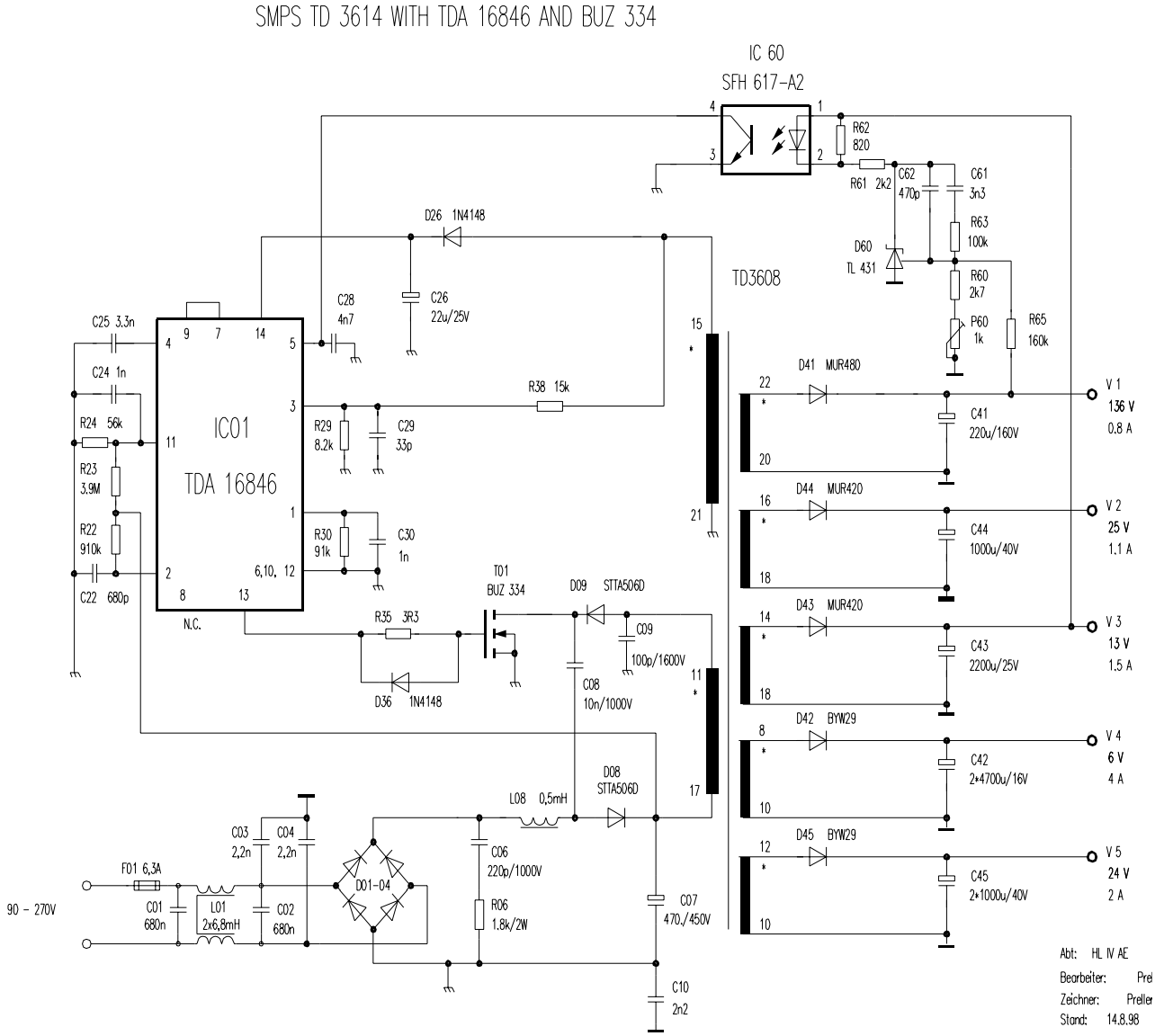

Fig. 24: SMPS for TV- High End

SMPS Application for VCR- set (30 W, TD 3594)

The circuit is shown in Fig. 25. This SMPS is designed for low output power without PFC but with an opto coupler. The controlled voltage is V3 (6V) because this voltage has a very narrow tolerance for this application. The snubber circuit consists of the diode D08 (BYT 52M) and two 100 V Zener diodes D27 and D28. With the serial connection of Zener diodes the cut off voltage is the sum of the single voltages of the Zener diodes and the power dissipation is split according to the voltages. For more information about snubber circuits refer to chapter 7.

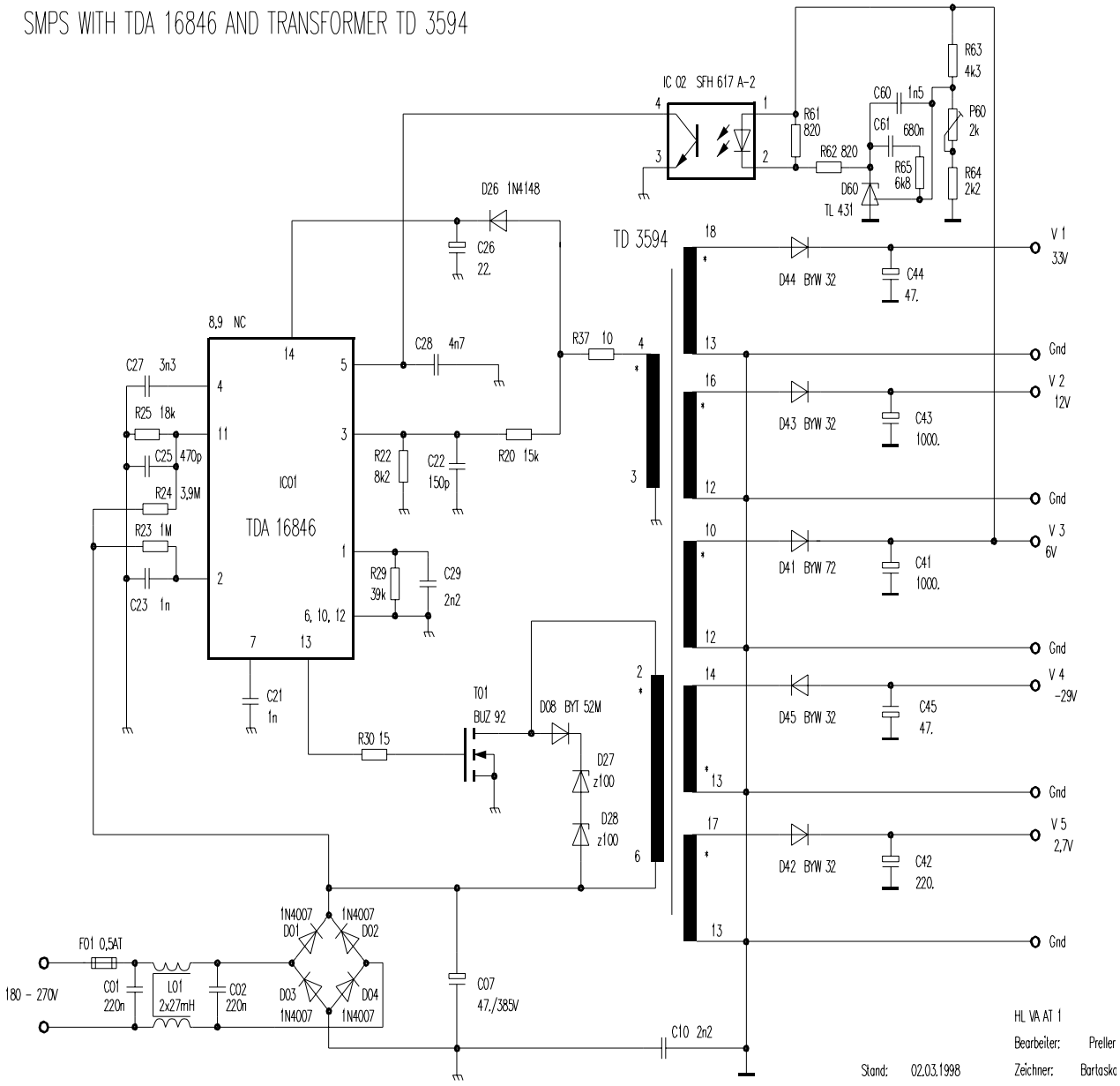

Fig. 25: SMPS Application for VCR- Set

9. Applications for Fixed Frequency and Synchronized Mode

SMPS Application for fixed frequency mode (TD 3618)

The TDA 1684X can be programmed for fixed frequency mode with an external RC circuit at pin 7 as shown in Fig. 26. R21 and C21 determine the fixed frequency. The commonly used shunt resistor in fixed frequency mode between source of the MOS FET (T01) and ground is not necessary because the TDA 1684X uses current simulation (pin 2). Also in fixed frequency mode before the next switch on a zero crossing signal is necessary to avoid saturation of the transformer.

Naturally with a fixed frequency SMPS the switching on can take place not only at the minimum of the drain voltage, because the switching frequency is the fixed and the switch on time can not be set to the transformer oscillations. The transformer oscillations are also energy oscillations and can disturb the regulation in fixed frequency mode. A remedy for occasionally occuring irregularities of the switch on time is reducing the control loop bandwidth. The control bandwidth is determined mainly by the feed back circuit beween cathode and gate of the reference component D60 (R63, C61) and the capacitor at pin 5 of TDA 1684X.

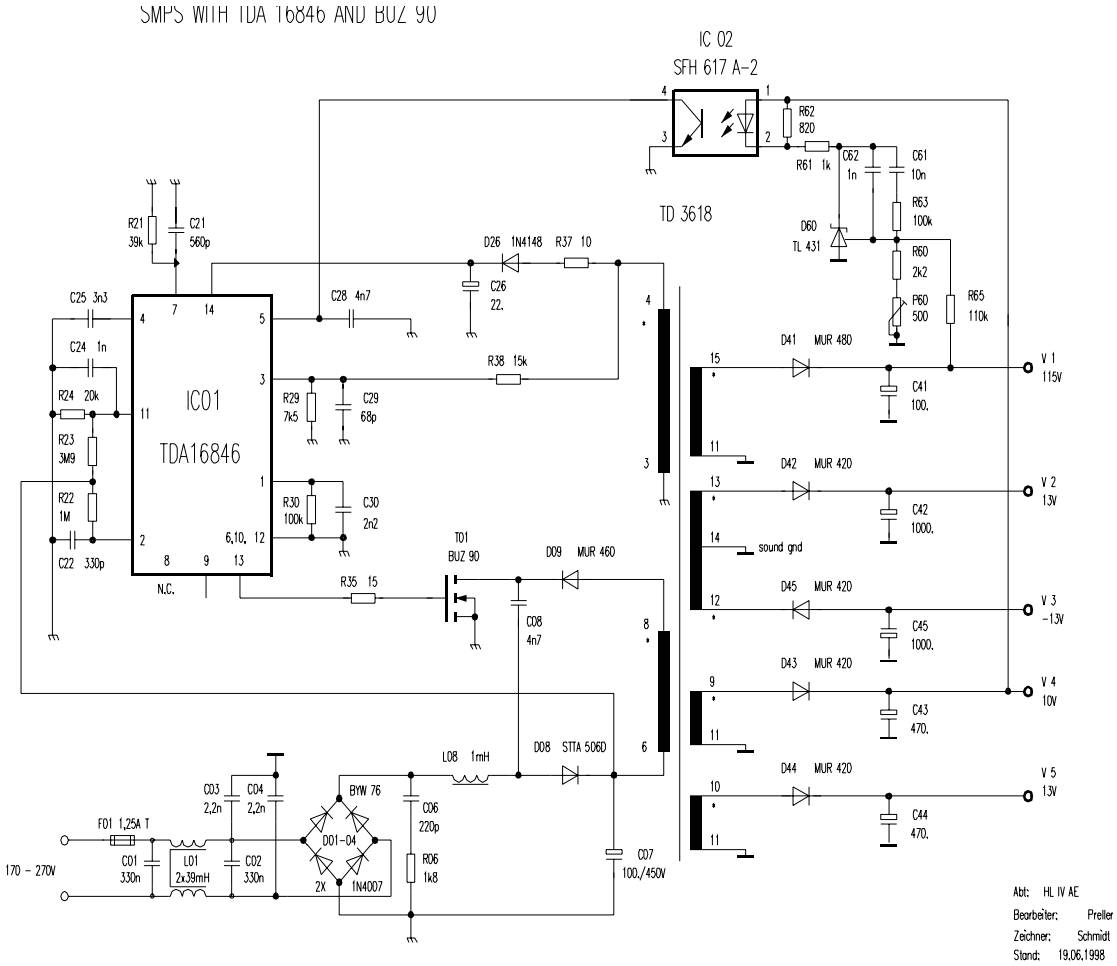

Fig. 26: SMPS Application for Fixed Frequency Mode

SMPS application for synchronized mode (TD 3628)

Fig. 27 shows an SMPS for fixed frequency and synchronized mode. Additionally, an opto coupler IC 03 (SFH 617 A-2) is connected to the external RC- circuit at pin 7 across the diode D50, the transistor T50 and the base resistor R50. Changes of the collector- emitter- voltage of the opto coupler output transistor are avoided by the transistor T50, resulting in a considerable enhancement of the switching speed. Therefore the synchronization can done without a fast and expensive high speed opto coupler. Since in synchronized mode only switching edges are important, the synchronizing pulses are fed capacitivly into the opto coupler via C51. The anti parallel diode D51 is mandatory. This capacitive drive results in a further increasement of the pulse transmission speed.

To reduce input power, the output voltages are lowered in standby mode. The lowered value is determined by the Zener diode D62 between the output voltage V3 and pin 1 of the opto coupler IC02. To avoid the condition that the supply voltage of TDA 1684X (IC01) at pin 14 doesn´t reach the switch off threshold (8V) during standby mode with heavy lowered output voltages, the supply voltage is partly stabilized: The voltage after the rectifying diode D31 is first smoothed by the elcap C31 (1µF). Connected at C31 is a voltage divider, consisting of the resistors R31 and R29. An additional Zener diode D29 (10V) is serial connected to R29. The diode D26 prevents that during startup the startup current is flowing through R29 and D29 that would made a startup impossible. The number of turns of the control winding is set relatively high (10 turns with 2.7 V per turn) so that in standby mode with lowered voltages the voltage at pin 14 lies clear above the undervoltage switch off value. The voltage at point R29 / R31 amounts then to approximately 10 V and the Zener diode D29 is still not conducting. The internal current consumption of the TDA 1684X of 5 mA causes a voltage drop of 1.5 V at the resistor R31 (300 Ohm). As soon as the voltages are rising in normal mode the voltage at the point R29 / R31 rises above 10 V and the Zener diode D29 conducts. The voltage increase at C31 is divided with the ratio R29 / (R29 + R31) so that the voltage at pin 14 has a margin of 1 V from the overvoltage threshold of 16 V in normal mode. Since the voltage at pin 14 is not hard clamped, but is rising likewise with the rising output voltages, the overvoltage protection at pin 14 is not lost. The supply voltage at pin 14 in normal mode can now lie closer at the overvoltage threshold, because the voltage rise of the supply voltage at pin 14 is slowed down.

In normal mode the power dissipation in R31 and D29 is higher because of the bleed off current flowing through them.

For switching between standby and normal mode a mechanical switch is provided at the ground sided terminal of the potentiometer P60 which can be replaced by a electronic switch during integration in the chassis. At opened switch the reference component TL 431 is connected directly and the output voltages drop to the value which is determined by the Zener diode D62.

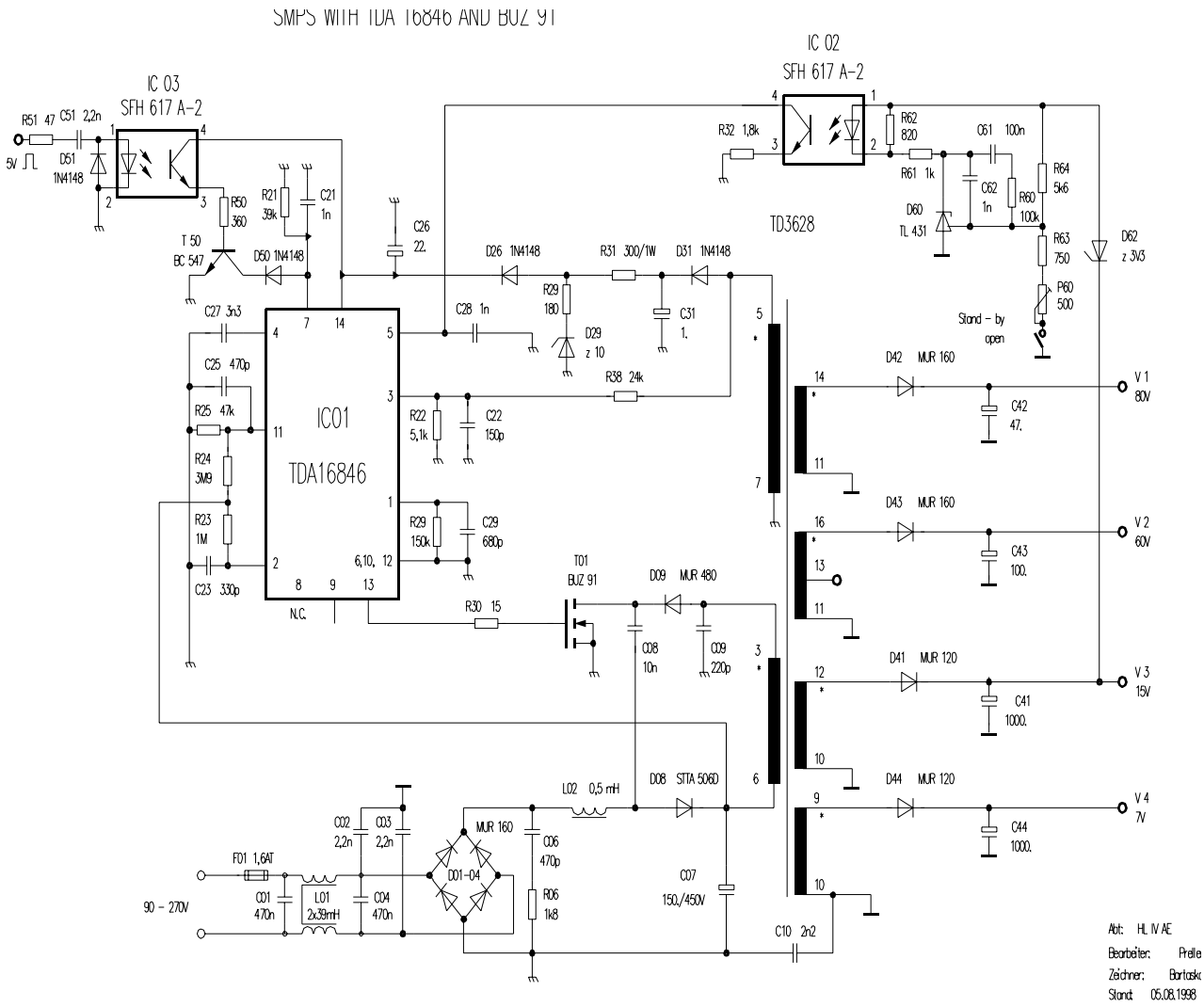

Fig. 27: SMPS Application for Synchronized Mode

10. Tips and Tricks

a) Hints for the Layout

A good layout for the SMPS is very important. Leads for high voltages and currents have to be separated from small signal leads for the control chip. Fig. 28 shows a SMPS circuit diagram which meets the EMV requirements. A common rule is that all ground lines are separated and are connected in 1 point (radial wiring). Then voltage drops at the leads cannot affect adjacent signals. It is also important that sensitive input signals from the control chip (primarily pins 1 to 5 of TDA 1684X) to the external components are as short as possible. Also ground leads can be used as screening for sensitive traces and can be laid out with large areas. Large foil areas also can be used as heat sinks.

Tip: We offer plain pcb boards with a tested layout for our customers.

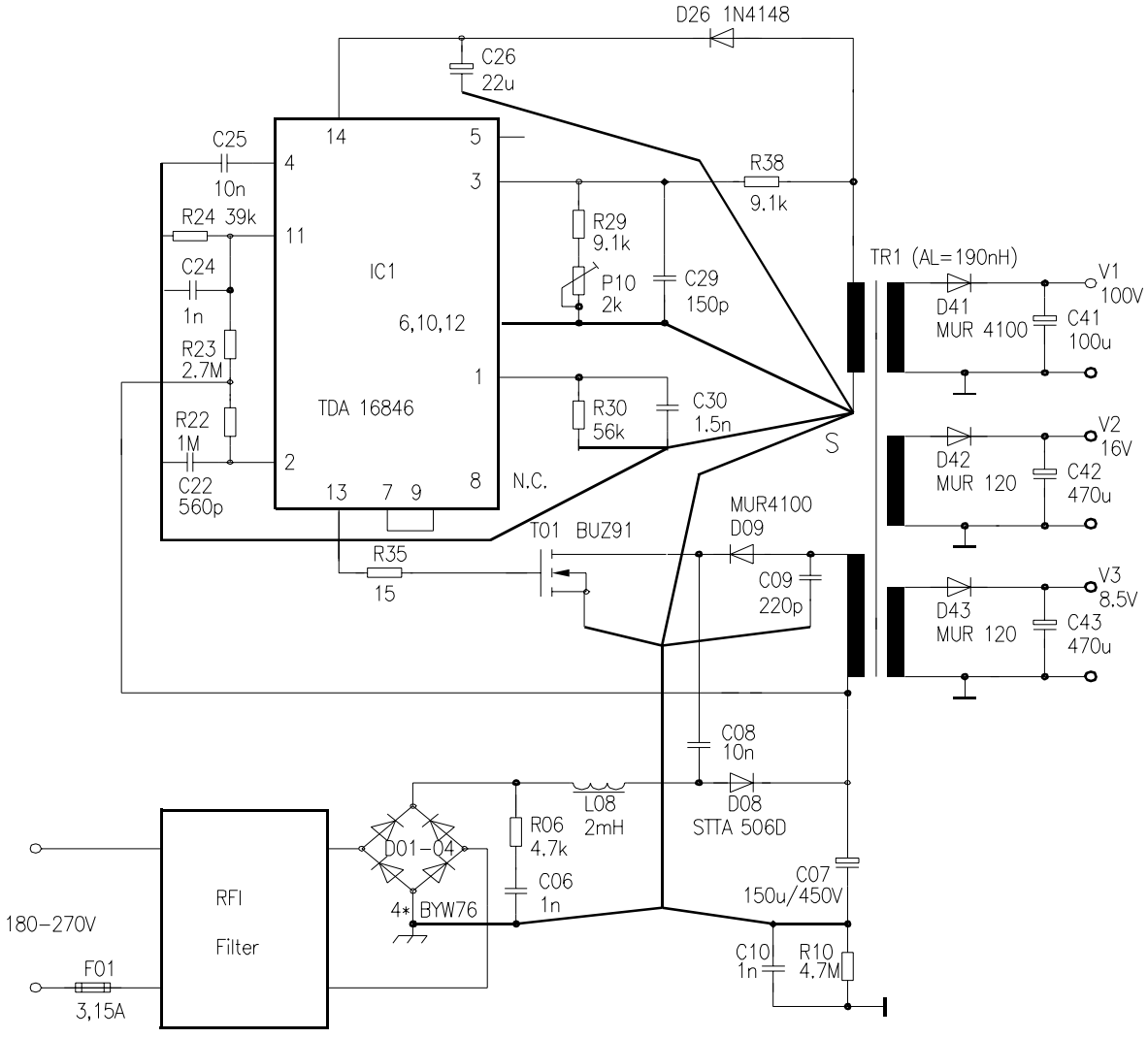

Fig. 28: SMPS Circuit Diagram According to Layout

b) Improving startup behaviour

Many problems with SMPSs are startup problems. During startup the supply voltage at pin 14 of TDA 1684X has to be observed. After reaching the 15 V threshold, the TDA 1684X switches to the operating current and the capacitor at pin 14 is discharged until the TDA1684X supply current is delivered from the transformer. At this time the supply voltage reaches it´s minimum which always should have a sufficient margin from the 8 V switch off level (at max. output load). If this margin is too small, the capacitor at pin 14 has to be made bigger or the output capacitors have to be made smaller. Startup can also be impossible when the fold back point is set too low (RC circuit at pin 2 too small).

If the highest secondary voltage V1 has no load during startup and the regulation is done by an opto coupler, a break can occur after charging the output capacitors and the supply voltage at pin 14 can reach the undervoltage switch off level during this break. As a remedy a Zener diode can be switched between the charged output voltage and the supply pin for the opto coupler. Then the break after startup is shortened and the charged output voltage and also the supply voltage for TDA 1684X is prevented from decreasing too far. An example for this method is shown in Fig. 22 (Zener diode D61 between V4 and pin 1 of SFH 617 A-2).

No noise should get into the primary voltage check input pin 11. Keep PCB power traces far away to prevent noise spikes at pin 11 from making startup impossible.

c) Stabilized supply voltage at pin 14. Especially at lowered output voltages in standby mode it can be necessary to stabilize partly the supply voltage at pin 14. For details s. chapter 9, Fig. 27.

d)

Lower Output Ripple

100/120 Hz ripple: When using primary regulation, the 100/120 Hz ripple can be lowered by optimizing the capacitor between pin 3 of TDA 1684X and ground. Also the coupling of the transformer has much influence. With secondary regulation the feed back circuit between cathode and gate of the reference IC TL 431 controls the output ripple.

High frequency- ripple (RF- noise): The RF- ripple at the output capacitors is dependent on the quality of the electrolytic capacitors (serial resistor ESR and inductivity). Lowering of the RF- ripple is possible by connecting several capacitors in parallel and by using low impedance ceramic bypass capacitors.

e) High Temperature

Excessive operating temperature of power components (MOS FET, diodes, transformer, chokes) can be lowered with

- bigger or additional heat sinks
- bigger and faster power components- lower $R_{DS(on)}$ MOSFET (Cool MOS), faster diodes
- more distance between power components
- larger layout area
- better convection cooling

f) Improved Transformer Coupling

Better coupling can be achieved by connecting windings in parallel (equal number of turns or equal inductance to avoid circulating currents) and interleaving the windings among each other.

Padding of the transformer: The innermost winding consists not of wire but of a certain number of isolation foils (layer type transformer). This method allows also lower temperature of the inner windings because of the bigger distance to the airgap (better effectivity).

Transformer type: The best coupling can be achieved with layer type transformers, followed by slot type and chamber type transformers.

g) Noise in the TV picture

Dots in the TV- picture caused by the SMPS RF- noise can be reduced by making the gate resistor of the power MOS FET higher. But with a higher resistor also the temperature of the MOS FET increases. A compromise has to be found. Improvement can also be achieved by modifying the snubber capacitor and the capacitors at the secondary diodes (capacitors between anode and ground instead between cathode and anode).

h) Change to PFC

A SMPS without PFC can be reconstructed for PFC by exchanging the snubber circuit (RCD) against the PFC charge pump circuit (LCD). The primary capacitor has to be exchanged by a type for higher voltage (450 V). The mains filter circuit has to be adapted (bigger X- capacitors and chokes). The regulation has to be checked (100 Hz ripple). See also chapter 3.

i) Remarks to some pins

Pin 1 (Off time circuit): The adjustment of the RC circuit at pin 1 should be performed in this sequence: First the rising time of the voltage at pin 1 has to be adjusted as described in the specification. After this is done, the standby frequency can be adjusted by the resistor between pin 1 and ground. Reason: The resistor has only little influence on the rising time of the voltage at pin 1, but the capacitor has influence on both the rising time and also the standby frequency.

The voltage at pin 1 V1 should not fall down completely to ground. This can happen during startup (long periods) when the RC circuit at pin 1 is reduced to shift the lowering of the SMPS frequency to smaller loads. If V1 gets too low, the startup can be interrupted. As a remedy a diode can be connected in series to the resistor between pin 1 and ground. Another solution is to connect an additional resistor between pin 1 and pin 9 (REF) so that a voltage divider between pin 9 and ground is formed.

Pin 2 (Primary current simulation PCS): The capacitor between pin 2 and ground must not be too big. After the switch on time of the MOSFET this capacitor is discharged by an internal current source of TDA 1684X. If the capacitor at pin 2 is too big, it may occur that it cannot be discharged completely until the next switch on time of the MOSFET. The result is that the regulation circuit increases the regulation voltage to get the same switch on time. Also the fold back point is lowered by this effect. The limit of the capacity of the capacitor at pin 2 depends on the SMPS frequency and the duty cycle.

Pin 5 (Opto coupler input): Pin 5 should not completely pulled to ground by the opto coupler. For correct working of the regulation circuit a distance of approx. 0.5 V between pin 5 and ground is needed. A diode or a 1.8 kOhm resistor in series between the optocoupler and ground ensures this distance if necessary.

Pin 11 (Primary voltage check): This pin is very sensitive towards short voltage spikes. A capacitor between pin 11 and ground (e.g. 10 nF) protects this pin against RF noise. Also a good layout is important which meets the EMC requirements.

Startup trials after switch off: Troublesome startups after switch off of the SMPS can be avoided by a bigger capacitor between pin 11 and ground (e.g. 100 nF). Then the discharging of the capacitor at pin 11 below the 1 V threshold is slower than the discharging of the primary capacitor and startups after switch off are impossible.

Delayed stop of running after switch off: After switch off in standby mode the SMPS is able to continue to work until the primary capacitor is discharged. For a faster stop of the SMPS it is recommended to connect the voltage divider for pin 11 not to the DC voltage of the primary capacitor but to the AC mains voltage. The voltage divider has to be adapted to get the same input voltage range. Dependent on the voltage divider at pin 11 a capacitor of 1 or 2 µF between pin 11 and ground is necessary for a smooth DC voltage. Please find examples in application circuits in chapter 13.

Pin 14 (VCC): We recommend to switch parallel to the supply capacitor between pin 14 and ground a small additional capacitor (e.g. 100 nF) to lower the RF ripple of the supply voltage. This is shown in Fig. 34 where the capacitor C261 is switched parallel to the capacitor C26.

11. Transformer Calculation

The transformer for a SMPS can be calculated with the following formulas. First the maximum output power Poutmax has to be calculated as the sum of the products of the output voltages and max. output currents. The max. input power Pinmax is the quotient of the max. output power Poutmax and the efficiency Eff (equation 1). For the efficiency Eff a preliminary value of e.g. 80 % can be presumed.

8)

$$Pinmax = \frac{Poutmax}{Eff}$$

According to the calculated input power Pinmax a suitable transformer can be chosen. The values AL and Ae which are used in equation 12) can be seen in the data sheet of the transformer.

The DC voltage Vpmin at the primary capacitor at minimal AC mains voltage Vmmin is:

9)

$$Vpmin = Vmmin \times \sqrt{2} \times Fhum$$

Fhum = factor for the 100 Hz ripple at the primary capacitor. Fhum = 0.9.

The DC voltage Vpmax at the primary capacitor at maximal AC mains voltage Vmmax is:

10)

$$Vpmax = Vmmax \times \sqrt{2} \times Fcp$$

Fcp = factor for the overvoltage at the prim. capacitor. Without PFC: Fcp = 1, with PFC: Fcp = 1.1

The max. average current Ipmax through the primary winding is:

11)

$$Ipmax = \frac{Pinmax}{Vpmin}$$

Now the number of turns of the primary winding can be calculated with the formula:

12)

$$np = \frac{(Vdmax - Vpmax) \times Bmax \times Ae}{(Vpmin \times Fos + Vdmax - Vpmax) \times 2 \times Ipmax \times AL}$$

whereby

Vdmax = max. allowed drain voltage of the power MOS FET, e.g. 600 V

Bmax = max. allowed transformer core magnetization, e.g. Bmax = 300 mT

Fos = factor for the overshoots at the prim. winding. Without PFC: Fos = 1.3, with PFC: Fos = 1.8

The secondary voltage per turn Vts becomes:

13)

$$Vts = \frac{Vdmax - Vpmax}{np \times Fos}$$

Now the number of turns of the secondary windings and also the real output voltages can be calculated using the desired secondary voltages and the secondary voltage per turn Vts . If the calculated real output voltages don´t lay within the tolerances of the desired output voltages, a new attempt has to be made by setting a lower value for the magnetization Bmax and the calculation has to be restarted with equation 12).

The max. draincurrent of the power MOS FET Idmax becomes:

14

$$Idmax = Ipmax \times 2 \times \left(1 + \frac{Vpmin}{np \times Vts}\right)$$

The longest switch on time tonmax and the longest switch off time toffmax become:

115)

$$tonmax = \frac{AL \times (np)^2 \times Idmax}{Vpmin}$$

16)

$$toffmax = \frac{tonmax \times Vpmin}{Vts \times np}$$

The lowest free running SMPS frequency fmin is then:

17)

$$fmin = \frac{1}{tonmax + toffmax}$$

If the SMPS frequency fmin is too low, e.g. below 20 kHz and in the audible range, the calculation has to be restarted with formula 12) and with a lower value for Bmax.

12. Standby Input Power of the 80 W Demoboard with TDA 16846

Diagram Fig. 29 shows the mains input power Pin in relationship to the output load Pout for the 80 W demoboard for TDA 16846. The board has been operated at 110 V and 230 V mains voltage and was modified with and without PFC charge pump circuit. A constant load resistor R1 = 270 kOhm was connected between V1 (100 V) and ground to prevent too high a voltage at this output. For the variable load a current I3 from 0 to 50 mA has been taken out from output V3 (8.5 V). The frequency was adjusted to 20 kHz.

The output power was calculated with the equation:

$$Pout = \frac{V1^2}{R1} + V3 \times I3$$

The result which can be seen in Fig. 29 is that the input power Pin in dependence of the output power Pout gets higher with higher mains voltage . The input power is also higher in the version with the PFC charge pump circuit. For better orientation the curve Pin = Pout is drawn in, which means 100 % efficiency.

In Fig. 30 the mains input power Pin at 230 V mains voltage and I3 = 30 mA can be seen in dependence of the standby frequency f which was shifted by changing the resistor R30 at pin 1 of TDA 16846. At output V1 a 270 kOhm resistor was connected to ground. As the output voltages also rise with the frequency (e.g. V1 rised from 132 V to 168 V in the circuit with PFC within the frequency range 10.8 kHz to 50 kHz), the output power (nominal 0.5 W) rose from 0.38 W to 0.53 W (I3 = const. = 30 mA). The result is that the input power climbs nearly linear with the SMPS frequency especially in the circuit with the PFC charge pump. So the standby frequency should be set as low as possible to save power.

One of the reasons for the higher input power in the version with PFC (Fig. 29 and Fig. 30) is surely the higher voltage at the primary capacitor C07 which causes higher switching losses. At 230 V mains voltage this voltage had a value of 356 V with PFC and was widely independent of the standby output power and the frequency. Without PFC this voltage was only 325 V.

In Fig. 31 and Fig. 32 the circuit diagrams of the power supplies used for this measurement can be seen. Fig. 31 shows the circuit diagram with PFC and Fig. 32 shows the circuit diagram with RCD snubber circuit instead of the PFC charge pump circuit.

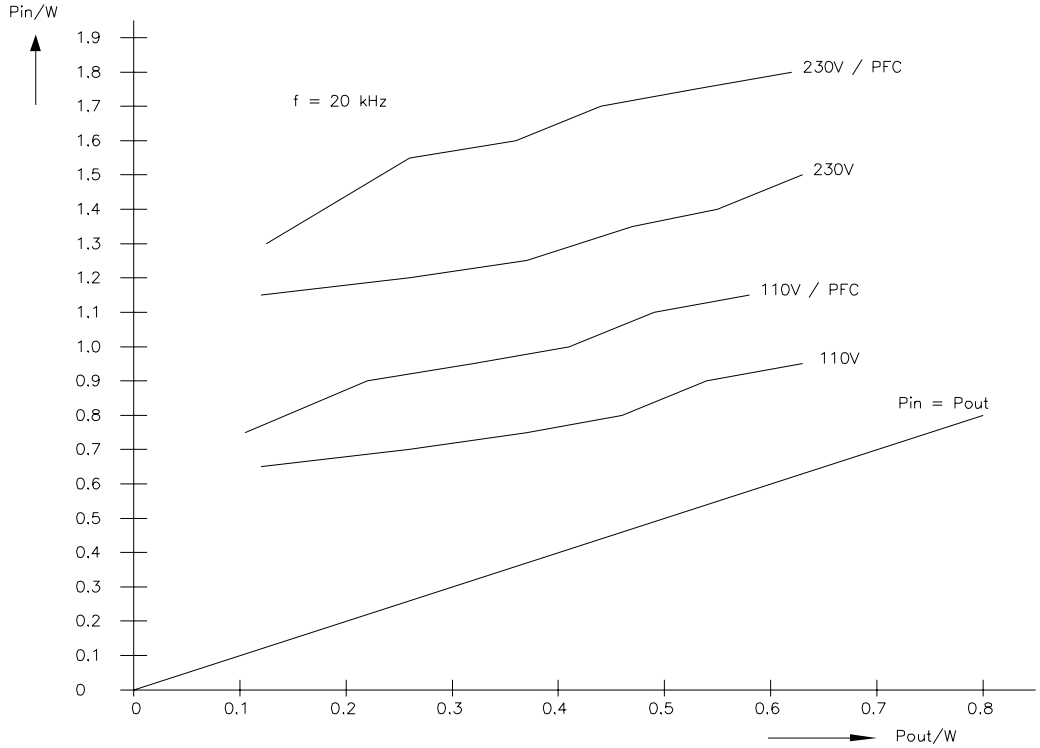

Fig. 29: Standby Input Power in Dependence of Output Power

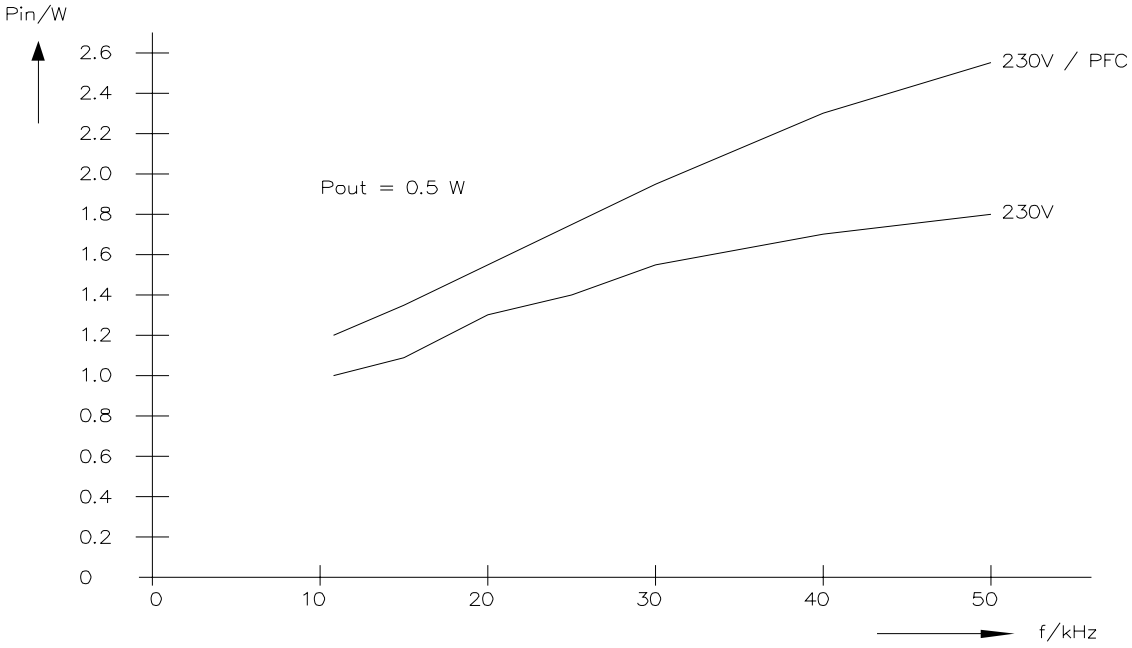

Fig. 30: Standby Input Power Pin in Dependence of the Frequency f

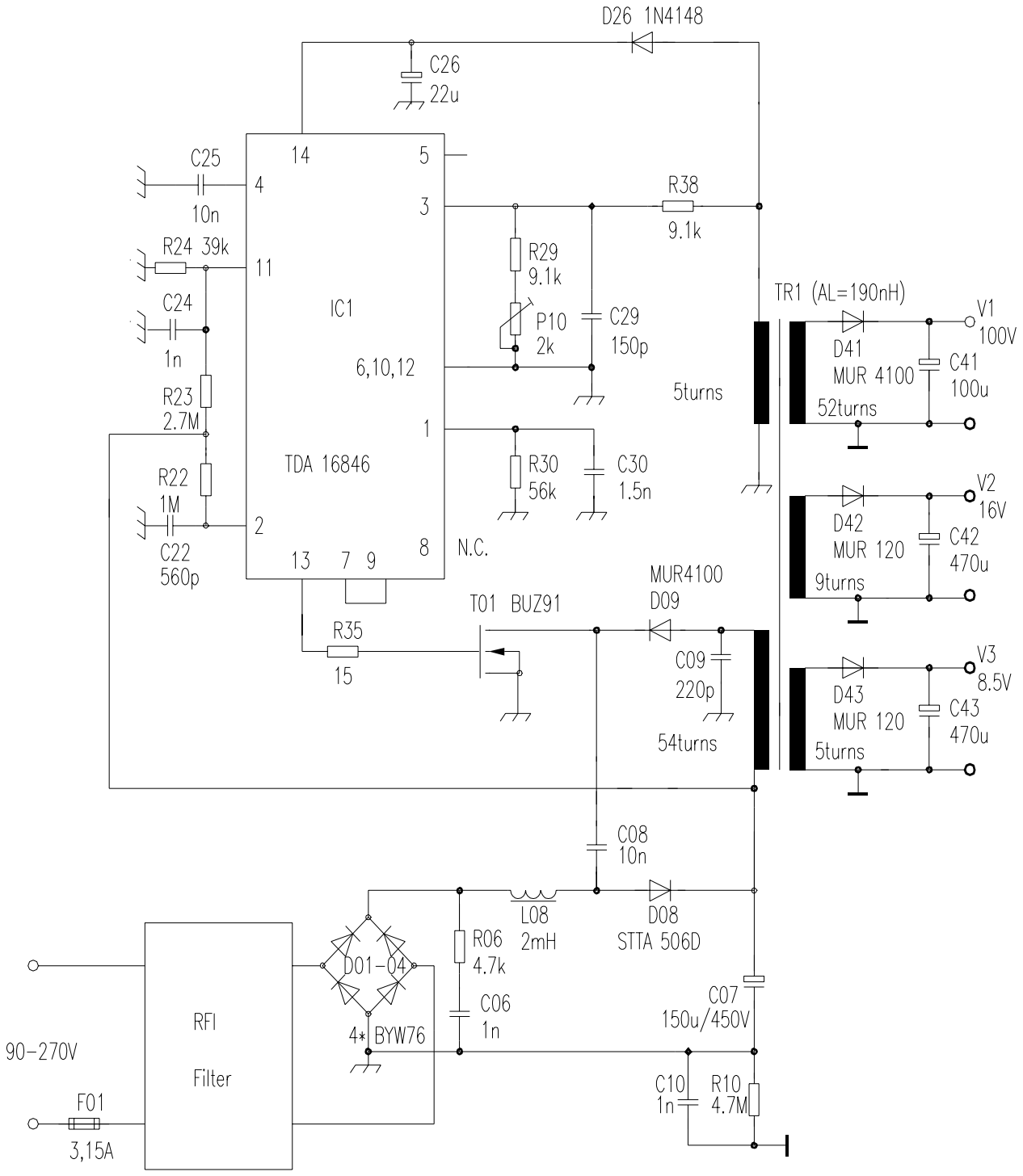

Fig. 31: Power Supply with TDA 16846 and PFC

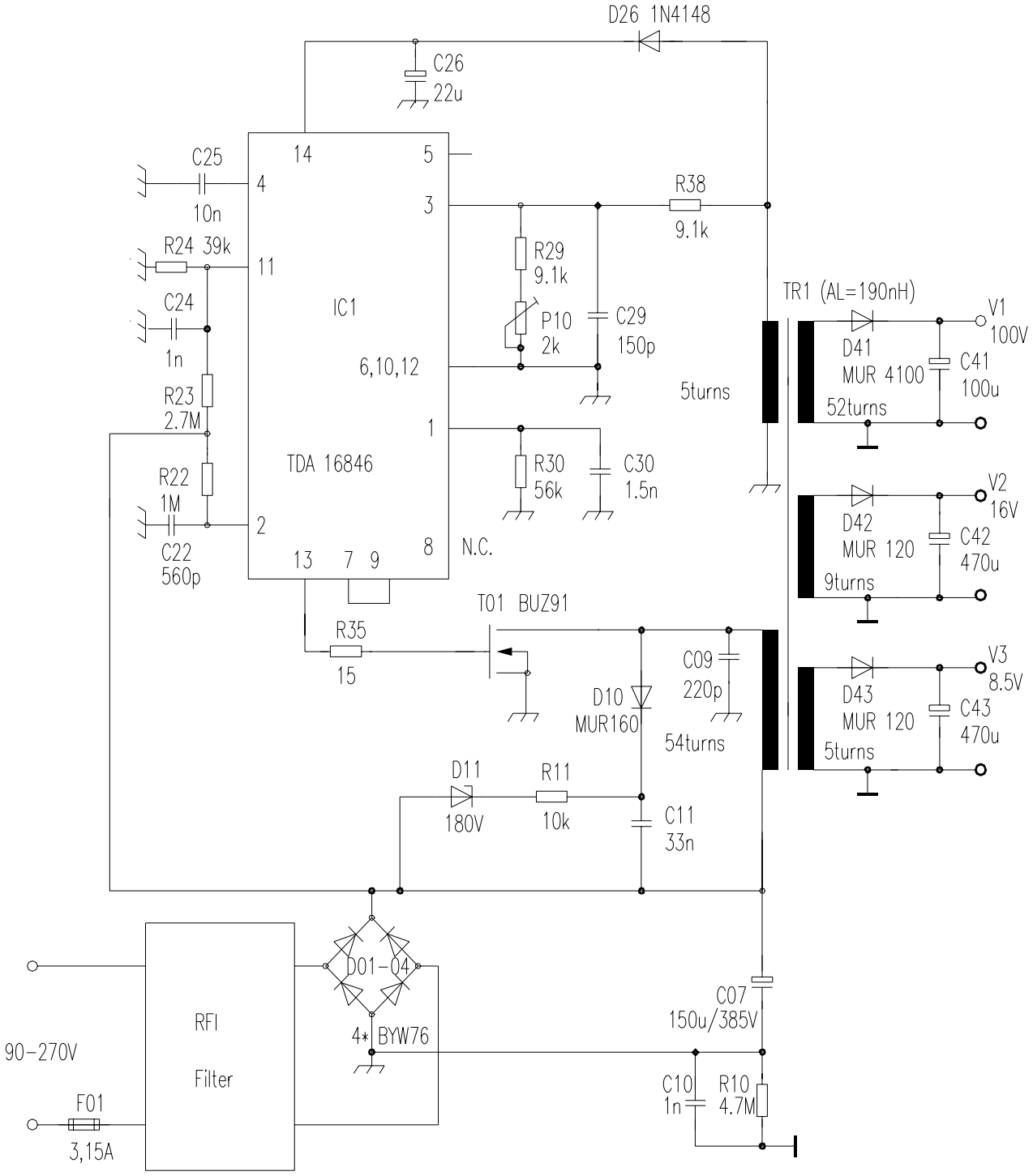

Fig. 32: Power Supply with TDA 16846 without PFC

13. New Application Circuits

13.1: 80 W SMPS TD 3622-2 with Primary Regulation and Standby Burst Mode

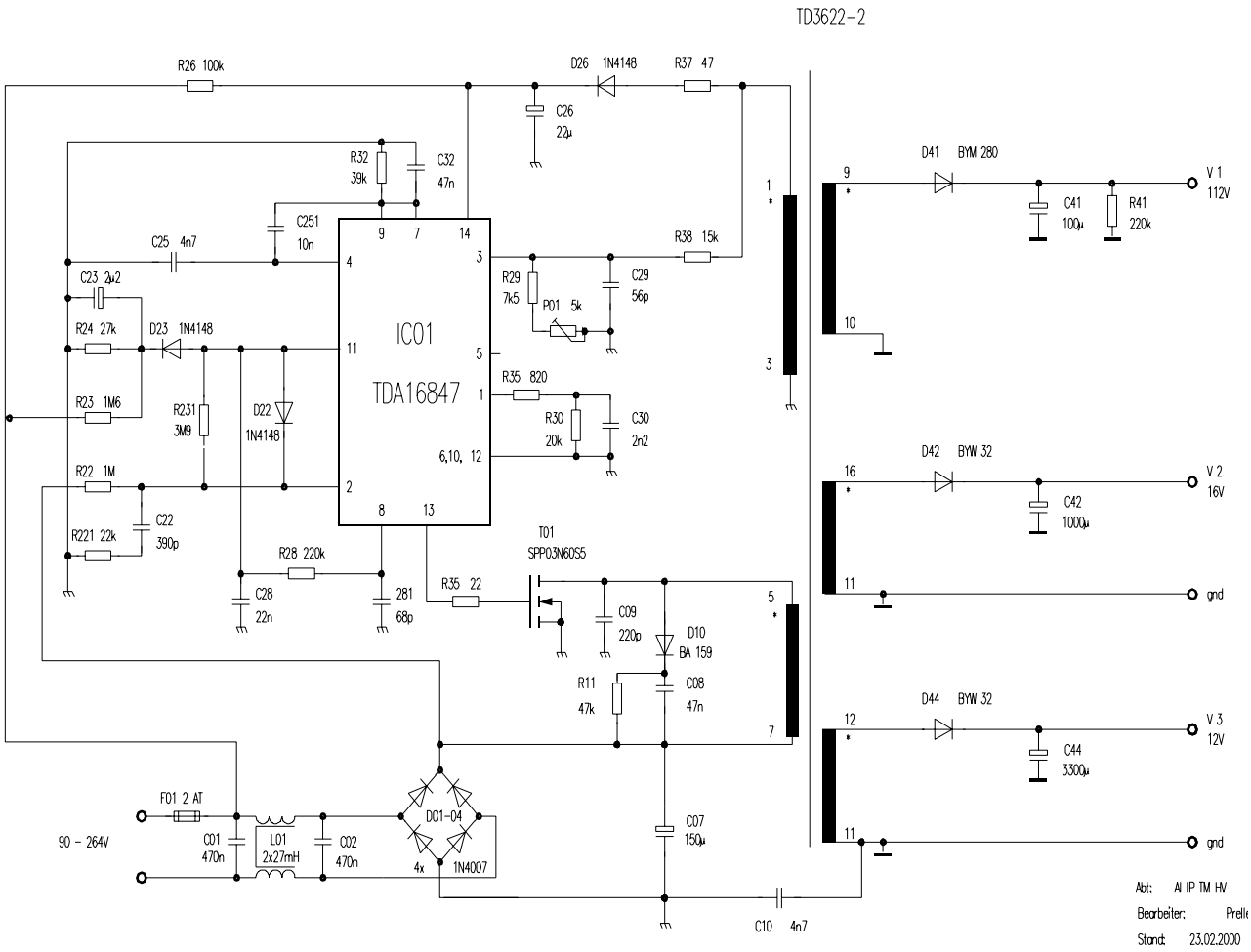

Fig. 33: SMPS with TDA 16847 with Standby Burst Mode and Primary Regulation

Description of SMPS TD 3622-2

Fig. 33 shows the SMPS TD 3622-2 which is primary regulated and without PFC charge pump circuit. With this SMPS a standby power consumption of 1.5W can be achieved with 425 mW output power at 230 V mains voltage and without demagnetization circuit (PTC- resistor). This low standby input power is reached with burst mode. The necessary differentiation between normal mode and standby mode is done by the power measurement circuit which is integrated in TDA 16847.

The output of the power measurement circuit is pin 8. A capacitor C281 is connected at pin 8 for building the saw tooth voltage dependent on the output power. This voltage is integrated and smoothed by the RC circuit R28 / C28. The DC voltage at C28 indicates the momentary power of the SMPS independent on the mains voltage. When the voltage at C28 goes below a certain limit, the SMPS has to switch into the standby burst mode.

This function is realized by connecting the capacitor C28 with pin 11, the input for the undervoltage lockout. At very low output power in standby mode the voltage at pin 11 falls below the threshold of 1 V and the SMPS switches off. After the supply voltage V14 falls below its undervoltage threshold 8 V, the TDA 16847 switches into startup mode and the capacitor C26 is charged again by the current through R26. After the starting voltage 15 V is reached at pin 14, the IC switches again into operation mode. So repetitive startups are performed at low output power. This kind of operation is called hiccup mode or burst mode.

Pin 11 acts now as comparator input for the actual power. The remaining problem is not to lose the other functions for which pin 11 is provided, namely the primary undervoltage lockout and the fold back point correction.

Undervoltage lockout: The voltage divider for the primary voltage R23 / R24 is separated from pin 11 by the diode D23. With this diode the pin 11 voltage can only be lowered but not heithened by the primary voltage. A high primary voltage cannot simulate a high power at pin 11 but a primary undervoltage is able to switch off the SMPS across the diode D23.

Fold back point correction: The integrated function of the fold back point correction is inhibited by the diode D22 between pin 11 and pin 2. The diode D22 limits the voltage at pin 11 to about 2 V to prevent a reducing of the fold back point caused by a high voltage of the power measurement circuit. The resistor R231 effects a precharge of the capacitor C28 during each startup.

The fold back point correction is done now by an additional resistor R221 between the capacitor C22 at pin 2 and ground. The resistor R221 causes a voltage drop during the charging time of C22 which is dependent on the primary voltage and thus the max. switch on time is reduced with increasing mains voltage. Thus the fold back point correction function is fulfilled.

The resistor R26 at pin 14 has to charge the capacitor C26 during startup and burst mode to get a higher burst repeat frequency. The additional capacitor C251 between pin 4 and pin 9 (reference voltage) forms a capacitive voltage divider with the capacitor C25 and causes a steep rise of the voltage at pin 4 at begin of each burst when the internal reference voltage is switched on. With this circuit the switch on time during the burst is tolerably constant. The resistor R32 at pin 9 is necessary to enable the power measurement circuit of TDA 16847. This resistor also determines the current out of pin 8. The additional capacitor C32 between pin 9 and ground smoothes the current through R32 and thus the current out of pin 8.

13.2: 200 W PFC Demoboard with Low Power Standby Burst Mode

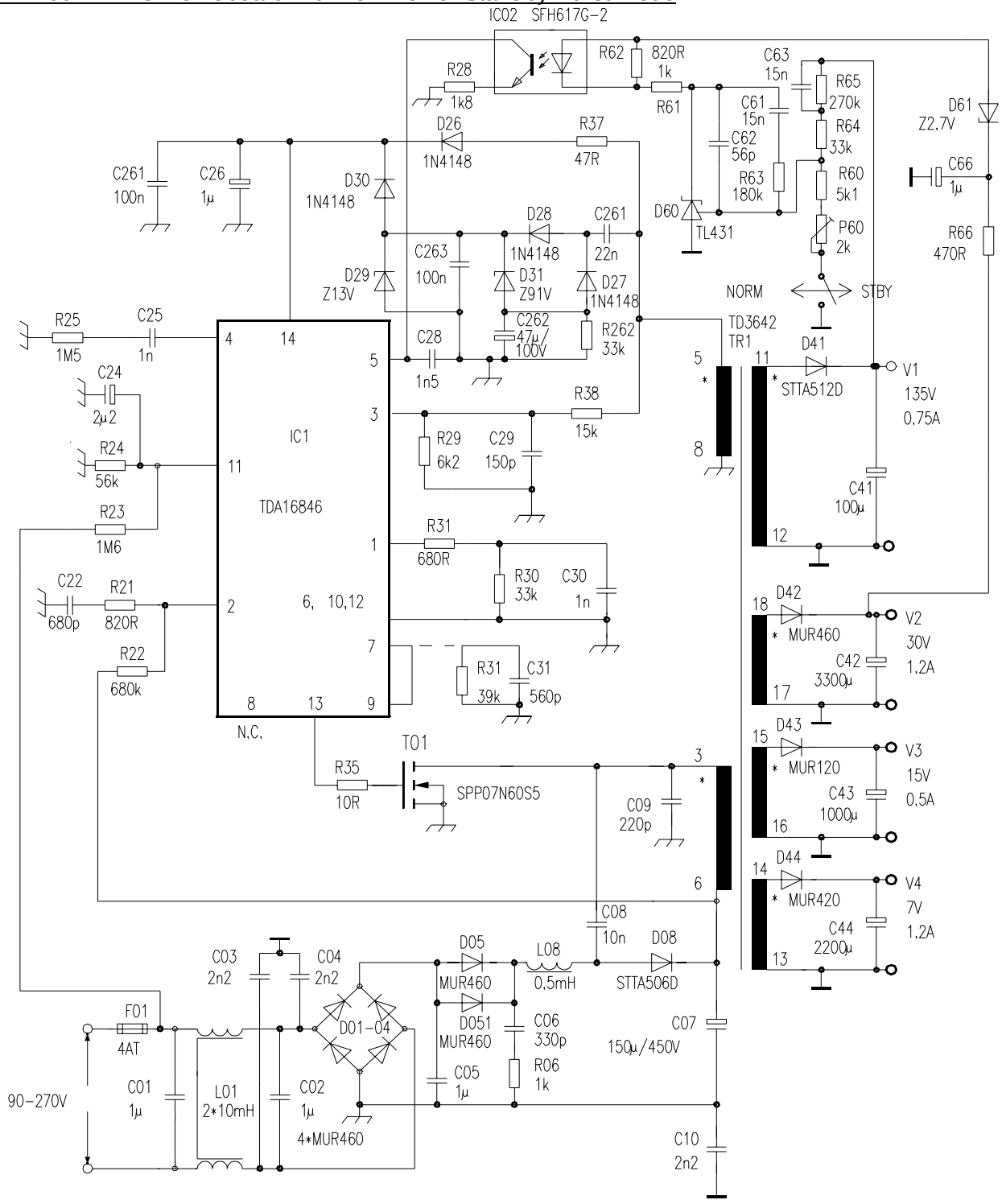

Fig. 34: 200 W SMPS Demoboard TD 3642 with PFC and Standby Burst Mode

20.06.2000

Description of the SMPS TD 3642

The SMPS TD 3642, whose circuit diagram is shown in Fig. 34, is a 200 W power supply especially for high end TV applications. It is equipped with a Charge Pump Circuit (L08, D08, C08) for Power Factor Correction (PFC) and a special low power standby burst mode circuit which makes only 1 W standby input power possible with 250 mW output power and at 230 V mains voltage.

In standby mode the output voltages are lowered to 25% of the value in normal mode. The lowered output voltages are the cause at primary side to switch into burst mode. The switching losses which are dependent on the voltage are reduced. This reduction of the output voltages is done by switching off the switch S1 at the bottom of the voltage divider for V1. The reference diode D60 becomes conducting and pin 5 of TDA 16846 is pulled down by the optocoupler. The output pulses at pin 13 are stopped and the output voltages are falling until the output V2, which has to be the supply output for the standby processor, has reached its low value which is determined by the Zener diode D61.

Burst mode consists of permanent startups (also called hiccup mode). To get very low input power, no additional startup resistor is used which would have its own power dissipation. The resistor R22 for the primary current simulation at pin 2 is also used as charging resistor for burst mode and has the high value 680 kOhm. To get a high burst repeat frequency in spite of the high charging resistor, the capacitor C26 at pin 14 is lowered from 22µF to 1µF.

During the burst the IC gets its supply voltage from a separate voltage supply circuit. The small capacitor C26 of only 1 µF cannot store enough energy to supply the IC during the burst and for the transition from standby to normal mode. The advantage of this supply circuit is that the supply voltage is produced only as long as it is needed and no supply energy is wasted. This circuit is realized by the charge pump circuit C261, D27 and D28 which is supplied in turn by the pulses of the transformer supply winding. The capacitor C263 smoothes the output voltage.

The output voltage is stabilized with the Zener diode D29 to 13 V. The diode D30 prevents that the current for charging C26 during startup is flowing backwards into the charge pump circuit. The anode of the diode D27 is not directly connected to ground but across a parallel RC circuit R262 / C262. This RC circuit allows operation of the charge pump circuit only for a short time. This is necessary to prevent overtemperature of the Zener diode D29 in normal mode and to make possible that the under voltage lockout function at pin 14 of TDA 16846 is still operative. The resistor R262 limits the current of the charge pump circuit in normal mode to max. 3 mA so that the IC cannot be supplied by this circuit permanently. As soon as the regulation stops the output pulses during the burst, the charge pump circuit stops to work and the storage capacitor C26 is discharged within short time. C26 is now charged by R22 for the next burst.

During normal mode, especially at high mains voltage and low output current, when the SMPS runs with high frequency, the charge pump circuit can produce a high negative voltage at the minus terminal of C262. This voltage is limited by the Zener diode D31 to protect the capacitor C262 and the diodes D27 and D28 from overvoltage.

The RC circuit R66 / C66 acts as a delay circuit for the optocoupler supply voltage. The effect is a total stop of the output pulses at the end of each burst because the voltage at C66 is still rising and produces current through the opto coupler after the regulation circuit has already regulated down. In this way after pulses are avoided, the burst is shortened to its effective part and switching losses are set to a minimum.

The RC circuit R25 / C25 at pin 4 shapes the regulation voltage in this way, that the switch on time during the burst is nearly constant. This is achieved by increasing the capacitor at pin 4. The resistor R25 causes a voltage drop at begin of the softstart current out of pin 4 and determines the starting value of the switch on pulses. With adjusting R25 and C25 an optimum can be found between power dissipation and noise in the transformer in standby burst mode. Bigger switch on pulses

cause lower power dissipation but also higher noise in the transformer.

To avoid jitter in TV applications (unstable periods) in normal mode which can cause distortions in the picture and noise in the transformer, lowering of the frequency is shifted below the normal load range.

The shift of the frequency path is done with 2 resistors: The resistor R31 at pin 1 of TDA 16846 and resistor R21 at pin 2 deform the voltage shapes at pin 1 and pin 2 in this way that the point of intersection between the regulation voltage and the voltage at pin 1 is shifted to a earlier time of the SMPS period so that switching on occurs at the first zero crossing signal within the normal load range.

In most PFC applications a diode between the drain of the MOS FET and the primary winding is necessary to avoid that current flows back into the primary winding and causes transformer oscillations with low frequency after the demagnetization of the transformer. This diode is not necessary in this application because the frequency is not reduced in normal mode. Also in fixed frequency mode and standby burst mode this diode is not necessary.

Fixed frequency mode: To switch into fixed frequency mode merely a RC circuit (R31 / C31) has to be connected to pin 7. The fixed frequency is set to a value which is higher than the lowest freerunning frequency (at max. output load and lowest mains voltage). So at high output load the operation of the SMPS is the same as in freerunning mode. When the output load is reduced, the SMPS continually changes into fixed frequency mode. The point of transition is reached when the freerunning period becomes as long as the fixed frequency period. The advantage is that in fixed frequency mode no less energy can be transmitted by the transformer as in freerunning mode.

Overload behaviour of SMPS TD3642

In Fig. 35 the overload behaviour of the SMPS TD3642 is shown. The output voltage V1 was measured in dependence on the output current I1 at 110 V and at 230 V mains voltage. The reason for the difference between both curves is, that at 230 V mains voltage the max. value of the regulation voltage of TDA 16846 is lowered because of the fold back point correction. So at 230 V mains voltage less current can be drawn out. To prevent switch off because of undervoltage during the measurement, the VCC pin 14 of TDA 16846 was supplied with an external voltage source. During the measurement only the V1 output was charged.

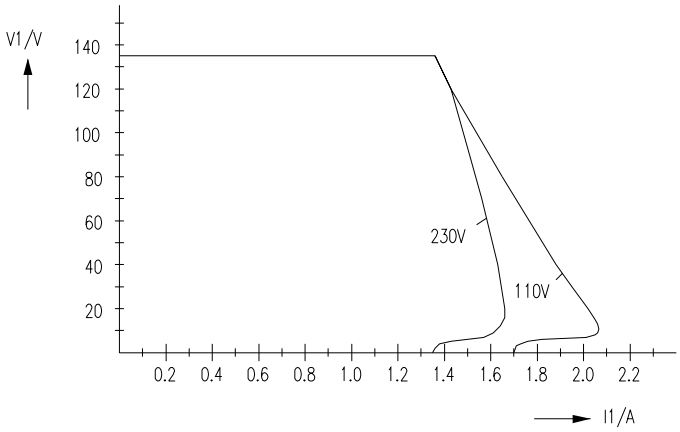

Fig. 35: Overload behaviour of SMPS TD3642_1

13.3: 115 W SMPS with Primary Regulation and lowered Voltages in Standby Mode

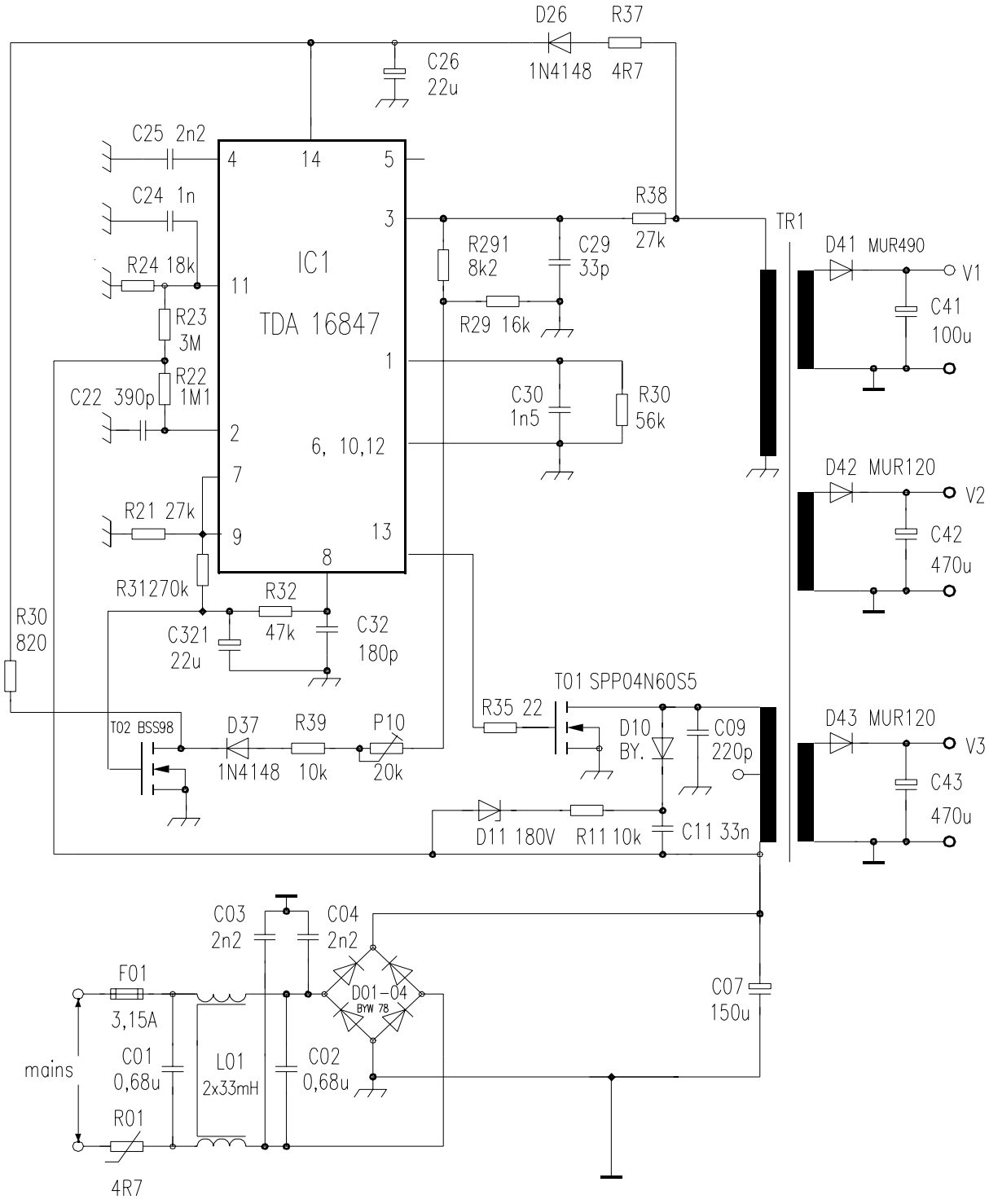

Fig. 36: SMPS with Primary Regulation and lowered Voltages in Standby Mode

21.06.2000

Description of the SMPS in Fig. 36

The circuit shown in Fig. 36 is a primary regulated 115 W SMPS with TDA 16847 and lowered output voltages in standby mode. An input power of 2.5 W can be achieved at an output power of 500 mW at 230 V mains voltage and without magnetization. The lowering of the output voltages in standby mode effects the low input power and prevents an overvoltage at the V1- output when only the low voltage outputs V2 and V3 are charged. The recognition between normal mode and standby mode is done by the integrated power measurement circuit in TDA 16847. The voltage at the capacitor C321 indicates the output power and controls the field effect transistor T02 (BSS98). In normal mode T02 is switched on and an additional pulse current is flowing through R291, P10, R39, D37 and T02. This current brings the output voltages to their normal values. They can be adjusted with the poti P10.

T02 also prevents the supply voltage V14 of TDA 16847 from overvoltage. When T02 is switched on in normal mode, V14 is charged with the resistor R30 (820 Ohm) and the voltage V14 is lowered. In standby mode T02 is switched off and V14 is uncharged to prevent undervoltage because of the lowered output voltages. The diode D37 blocks the reverse current between pin 14 and pin 3 because of the higher voltage at pin 14.

The advantage of the field effect transitor is that no base current is flowing that would cause a voltage drop across the resistor R32. The higher gate threshold voltage is compensated by the resistor R31 between pin 9 (5 V) and the gate of T02. The current through R31 causes a constant voltage drop across R32 to get a higher gate voltage.

The collector branch of T02 is not connected directly to pin 3 but to the tap of the voltage divider R291 / R29. With this method the power transition range between normal and lowered output voltages is narrowed because current from pin 3 through T02 flows only then when T02 is very good conducting. This is necessary when the distance between standby power and minimal power in normal mode is small or when a third kind of mode (copy mode) is implemented between standby and normal mode with switched off tube (only signal processing active). With this circuit the output voltages in standby mode and copy mode are completely lowered but have their normal values in normal mode.

13.4: Simple Kind of Burst Mode with TDA 16846

In Fig. 37 a SMPS circuit diagram with TDA 16846 and a simple kind of burst mode is shown. For the regulation an optocoupler (IC 60) is used. In normal mode the switch S1 between the poti P60 and ground is closed. To get into standby burst mode, the switch S1 (e.g. a transistor) has to be opened by a microprocessor. The reference diode D60 becomes full conducting and the output voltage V2, which is the used voltage for standby mode, falls down to a voltage which is determined by the Zener diode D61 and the minimal necessary supply voltage for the optocoupler and the reference diode D60 (TL431). At primary side the TDA 16846 can no longer supply itself because of the lowered transformer voltages and goes into a hiccup mode (repetitive startups). To get a higher burst repeat frequency and so a lower output ripple of the voltage V2, the charging of the supply capacitor C26 is quickened by the resistor R26 (100 kOhm) between pin 14 and the AC input.

Also with this burst mode the standby input power can be lowered noticeable.

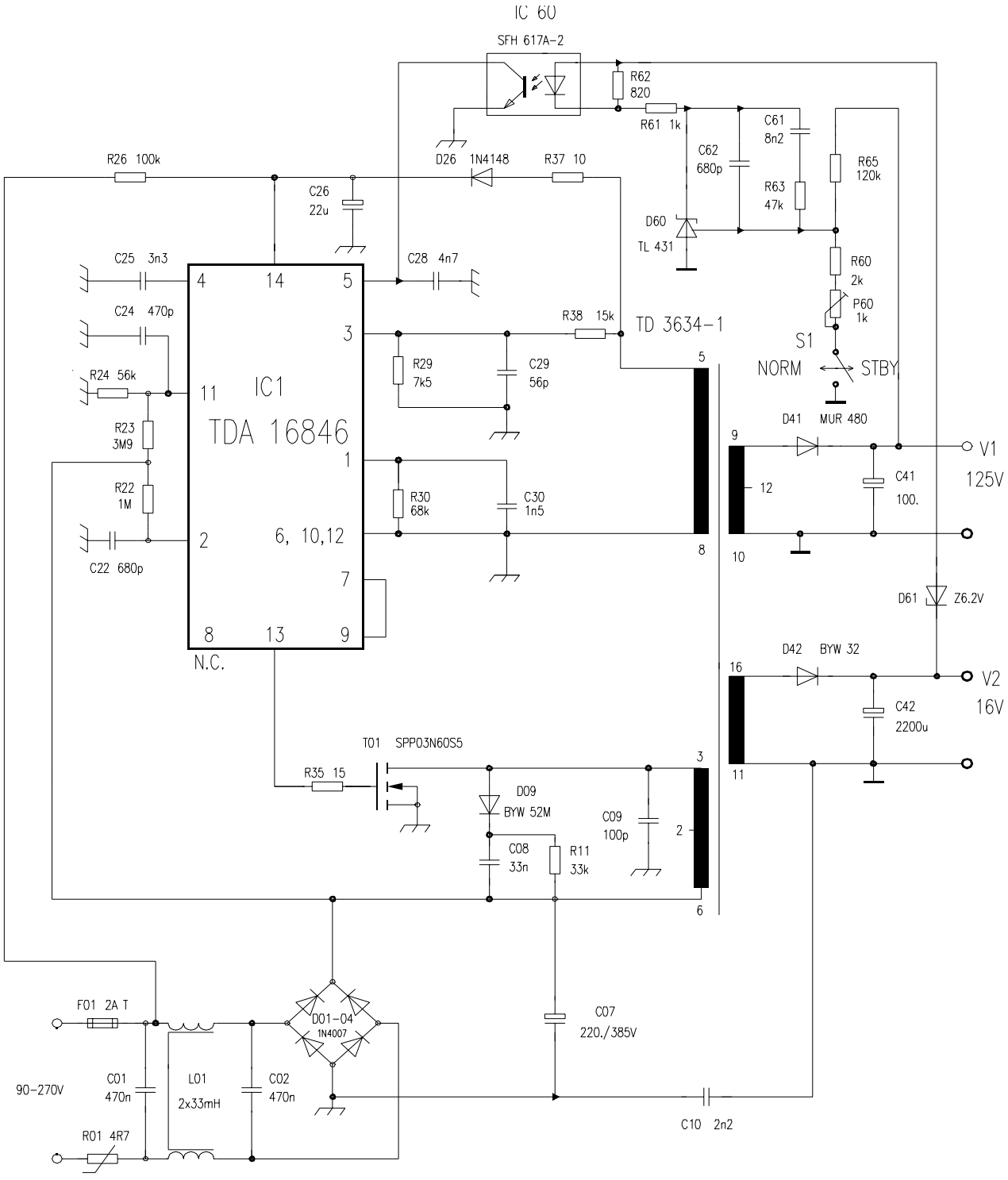

Fig. 37: Simple Kind of Burst Mode with TDA 16846

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Pacific,Pte.Ltd.
168 Kallang Way
Singapore 349 253
T (+65)8 40 06 10
Fax (+65)7 42 62 39
USA
Infineon Technologies Corporation
1730 North First Street
San Jose,CA 95112
T (+1)4 08-5 01 60 00
Fax (+1)4 08-5 01 24 24
Siemens Components,Inc.
Optoelectronics Division
19000 Homestead Road
Cupertino,CA 95014
T (+1)4 08-2 57 79 10
Fax (+1)4 08-7 25 34 39
Siemens Components,Inc.
Special Products Division
186 Wood Avenue South
Iselin,NJ 08830-2770
T (+1)7 32-9 06 43 00
Fax (+1)7 32-6 32 28 30
VRC
Infineon Technologies
Hong Kong Ltd.
Beijing Office
Room 2106,Building A
Vantone New World Plaza
No.2 Fu Cheng Men Wai Da Jie
Jie
100037 Beijing
T (+86)10 -68 57 90 -06,-07
Fax (+86)10 -68 57 90 08
Infineon Technologies
Hong Kong Ltd.
Chengdu Office
Room14J1,Jinyang Mansion
58 Tidu Street
Chengdu,
Sichuan Province 610 016
T (+86)28-6 61 54 46 /79 51
Fax (+86)28 -6 61 01 59
Infineon Technologies
Hong Kong Ltd.
Shanghai Office
Room1101,Lucky Target Square
No.500 Chengdu Road North
Shanghai 200003
T (+86)21-63 6126 18 /19
Fax (+86)21-63 61 11 67
Infineon Technologies
Hong Kong Ltd.
Shenzhen Office
Room 1502,Block A
Tian An International Building
Renim South Road
Shenzhen 518 005
T (+86)7 55 -2 28 91 04
Fax (+86)7 55-2 28 02 17
ZA
Siemens Ltd.
Components Division
P.O.B.3438
Halfway House 1685
T (+27)11-6 52 -27 02
Fax (+27)11-6 52 20 42