

FAST GATE TURN-OFF THYRISTORS

Thyristors in TO-220AB envelopes capable of being turned both on and off via the gate. They are suitable for use in high-frequency inverters, resonant power supplies, motor control, horizontal deflection systems etc. The devices have no reverse blocking capability. For reverse blocking operation use with a series diode, for reverse conducting operation use with an anti parallel diode.

QUICK REFERENCE DATA

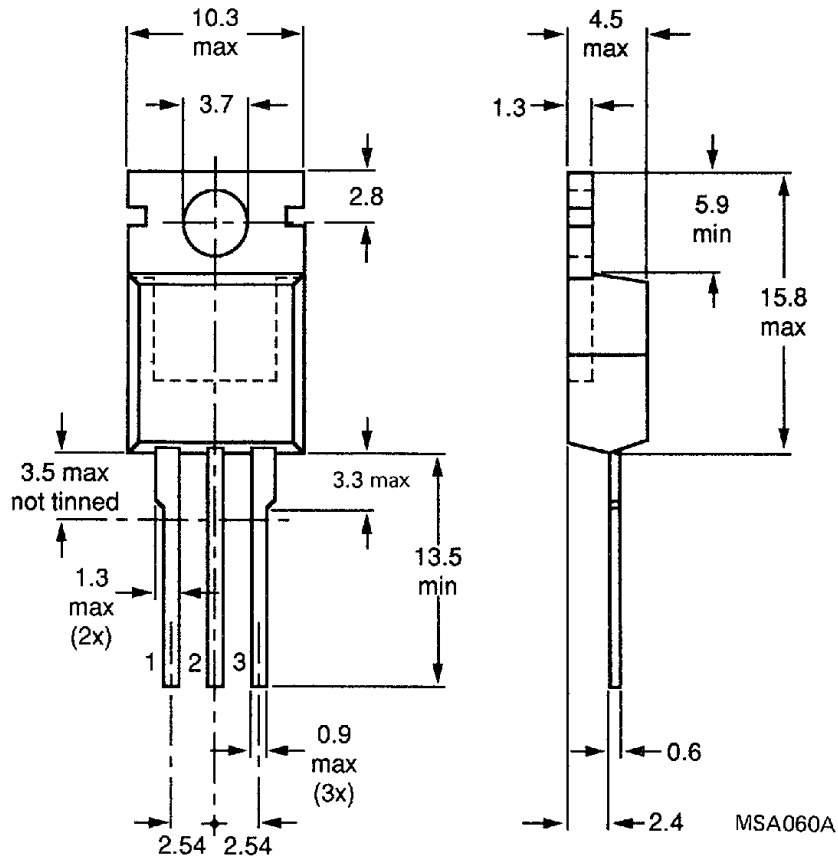
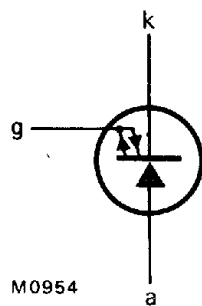
		BTW58-1000R			1300R	1500R	
Repetitive peak off-state voltage	V_{DRM}	max.	1000	1300	1500		V
Non-repetitive peak on-state current	I_{TSM}	max.				50	A
Controllable anode current	I_{TCRM}	max.				25	A
Average on-state current	$I_{T(AV)}$	max.				6.5	A
Fall time	t_f	<				250	ns

MECHANICAL DATA

Dimensions in mm

Fig.1 TO-220AB

- Pinning:
 1 = Cathode
 2 = Anode
 3 = Gate



Net mass: 2 g

Note: The exposed metal mounting base is directly connected to the anode.

Accessories supplied on request: see data sheets Mounting instructions and accessories for TO-220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Anode to cathode

			BTW58-1000R	1300R	1500R	
Transient off-state voltage	V_{DSM}	max.	1200	1500	1650	V*
Repetitive peak off-state voltage	V_{DRM}	max.	1000	1300	1500	V*
Working off-state voltage	V_{DW}	max.	650	1200	1300	V*
Continuous off-state voltage	V_D	max.	650	750	800	V*
Average on-state current (averaged over any 20 ms period) up to $T_{mb} = 85\text{ }^{\circ}\text{C}$			$I_T(AV)$	max.	6.5	A
Controllable anode current			I_{TCRM}	max.	25	A
Non-repetitive peak on-state current t = 10 ms; half-sinewave; $T_j = 120\text{ }^{\circ}\text{C}$ prior to surge			I_{TSM}	max.	50	A
I^2t for fusing; t = 10 ms			I^2t	max.	12.5	A ² s
Total power dissipation up to $T_{mb} = 25\text{ }^{\circ}\text{C}$			P_{tot}	max.	65	W

Gate to cathode

Repetitive peak on-state current $T_j = 120\text{ }^{\circ}\text{C}$ prior to surge gate-cathode forward; t = 10 ms; half-sinewave			I_{GFM}	max.	25	A
gate-cathode reverse; t = 20 μ s			I_{GRM}	max.	25	A
Average power dissipation (averaged over any 20 ms period)			$P_{G(AV)}$	max.	2.5	W

Temperatures

Storage temperature	T_{stg}		-40 to +150	$^{\circ}\text{C}$
Operating junction temperature	T_j	max.	120	$^{\circ}\text{C}$

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j-mb}$	=	1.5	K/W
From mounting base to heatsink with heatsink compound	$R_{th\ mb-h}$	=	0.3	K/W
with 56367 alumina insulator and heatsink compound (clip-mounted)	$R_{th\ mb-h}$	=	0.8	K/W

*Measured with gate-cathode connected together.

CHARACTERISTICS**Anode to cathode**

On-state voltage

$I_T = 5 \text{ A}; I_G = 0.2 \text{ A}; T_j = 120 \text{ }^\circ\text{C}$

$V_T < 3.0 \text{ V}^*$

Rate of rise of off-state voltage that will not trigger any off-state device; exponential method

$V_D = 2/3 V_{Dmax}; V_{GR} = 5 \text{ V}; T_j = 120 \text{ }^\circ\text{C}$

$dV_D/dt < 10 \text{ kV}/\mu\text{s}$

Rate of rise of off-state voltage that will not trigger any device following conduction, linear method

$I_T = 5 \text{ A}; V_D = V_{DRMmax}; V_{GR} = 10 \text{ V}; T_j = 120 \text{ }^\circ\text{C}$

$dV_D/dt < 1.5 \text{ kV}/\mu\text{s}$

Off-state current

$V_D = V_{Dmax}; T_j = 120 \text{ }^\circ\text{C}$

$I_D < 3.0 \text{ mA}$

Latching current; $T_j = 25 \text{ }^\circ\text{C}$

$I_L \text{ typ. } 1.0 \text{ A}^{**}$

Gate to cathode

Voltage that will trigger all devices

$V_D = 12 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

$V_{GT} > 1.5 \text{ V}$

Current that will trigger all devices

$V_D = 12 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

$I_{GT} > 200 \text{ mA}$

Minimum reverse breakdown voltage

$I_{GR} = 1.0 \text{ mA}$

$V_{(BR)GR} > 10 \text{ V}$

Switching characteristics (resistive load)Turn-on when switched to $I_T = 5 \text{ A}$ from $V_D = 250 \text{ V}$

$I_{GF} = 0.5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$

delay time

$t_d < 0.25 \mu\text{s}$

rise time

$t_r < 1.0 \mu\text{s}$

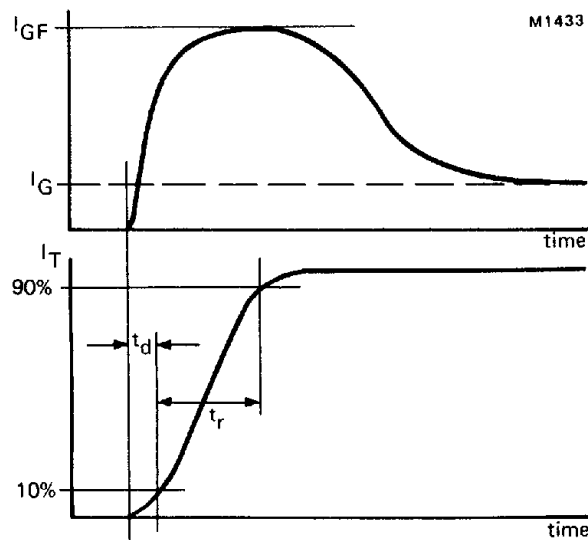


Fig.2 Waveforms

* Measured under pulse conditions to avoid excessive dissipation.

** Below latching level the device behaves like a transistor with a gain dependent on current.

Switching characteristics (inductive load)

Turn-off when switched from $I_T = 5 \text{ A}$ to $V_D = V_{DRMmax}$.

$V_{GR} = 10 \text{ V}$; $L_G \leq 1.0 \mu\text{H}$; $L_S \leq 0.25 \mu\text{H}$; $T_j = 25 \text{ }^\circ\text{C}$

storage time	t_s	<	0.5	μs
fall time	t_f	<	0.25	μs
peak reverse gate current	I_{GR}	<	6	A

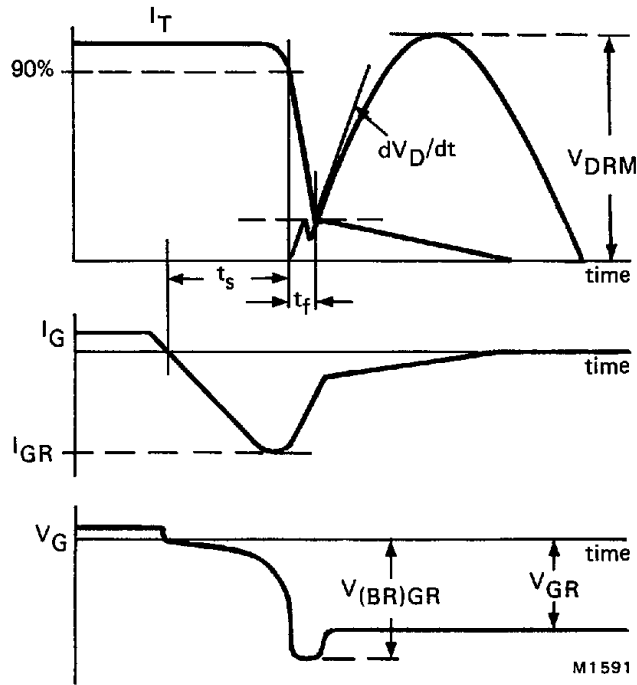


Fig.3 Waveforms.

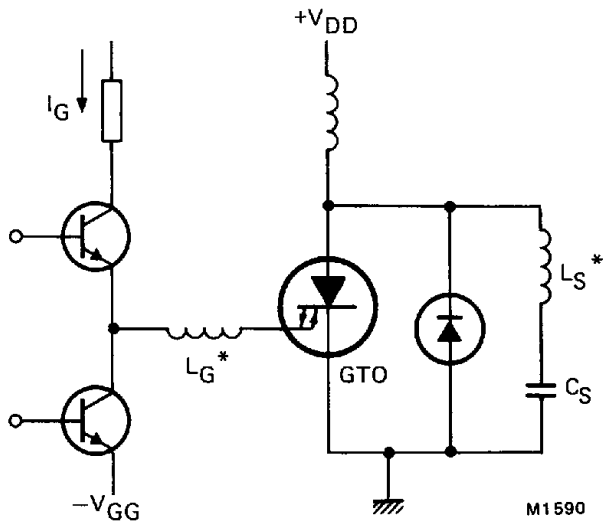


Fig.4 Inductive load test circuit

*Indicates stray series inductance only.

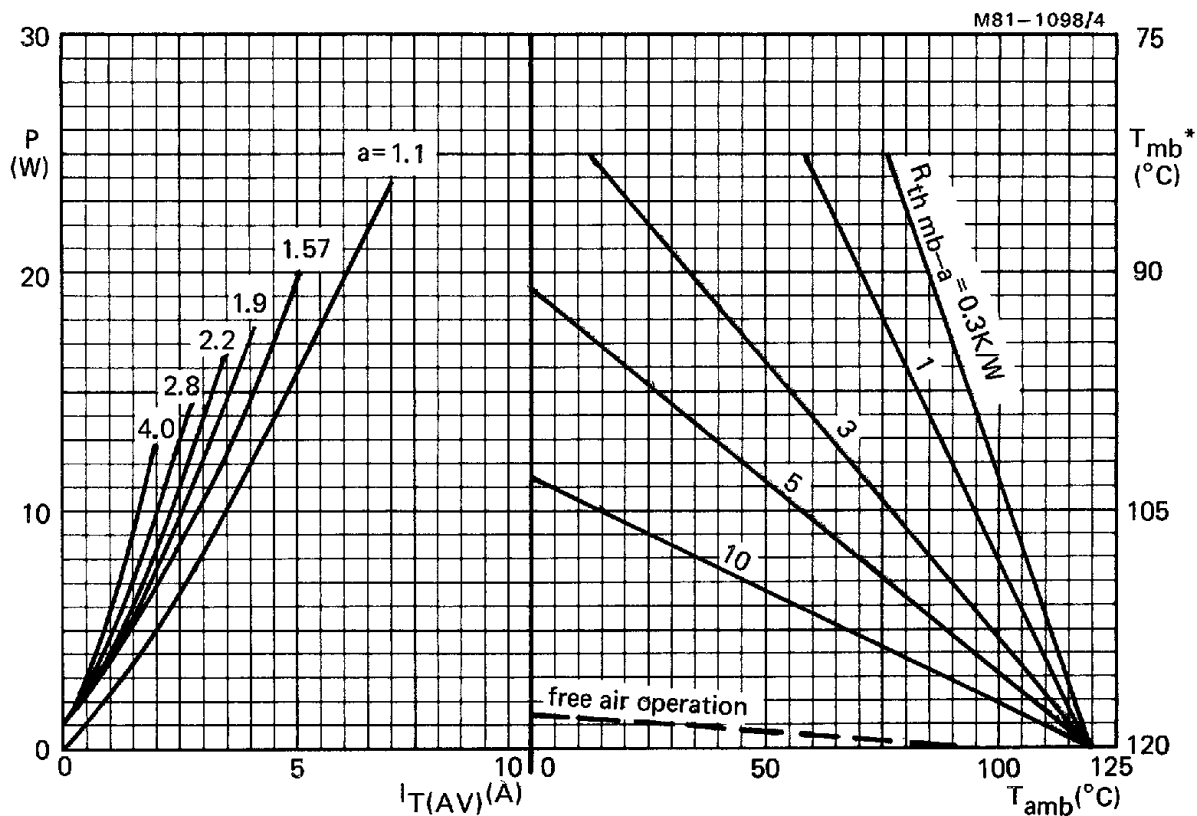


Fig.5 The right-hand part shows the interrelationship between the power (derived from the left-hand part) and the maximum permissible temperatures.

$$a = \text{form factor} = \frac{I_T(\text{RMS})}{I_T(\text{AV})}$$

P = power excluding switching losses.

*T_{mb} scale is for comparison purposes and is correct only for R_{th mb-a} < 9.6 K/W.

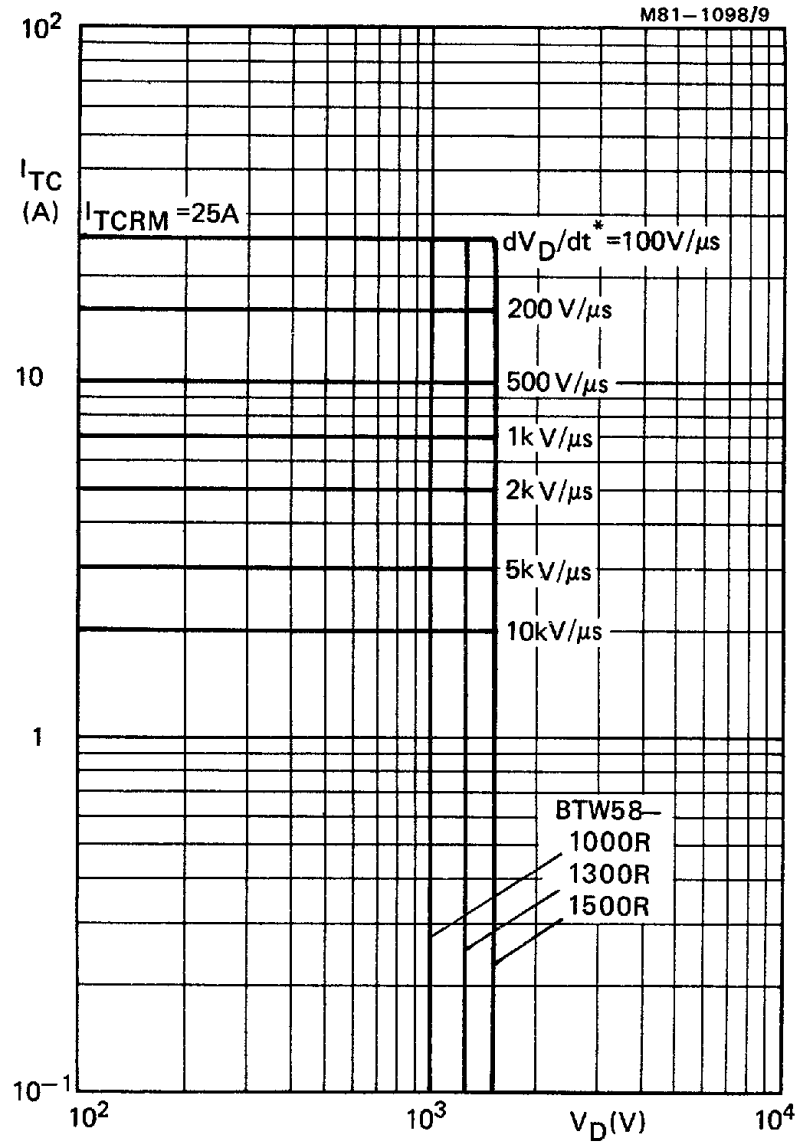


Fig.6 Anode current which can be turned off versus anode voltage; inductive load; $V_{GR} = 10 V$; $L_G \leq 1.0 \mu H$; $L_S \leq 0.25 \mu H$; $T_j = 85 \text{ }^\circ C$.
* dV_D/dt is calculated from I_T/C_S .

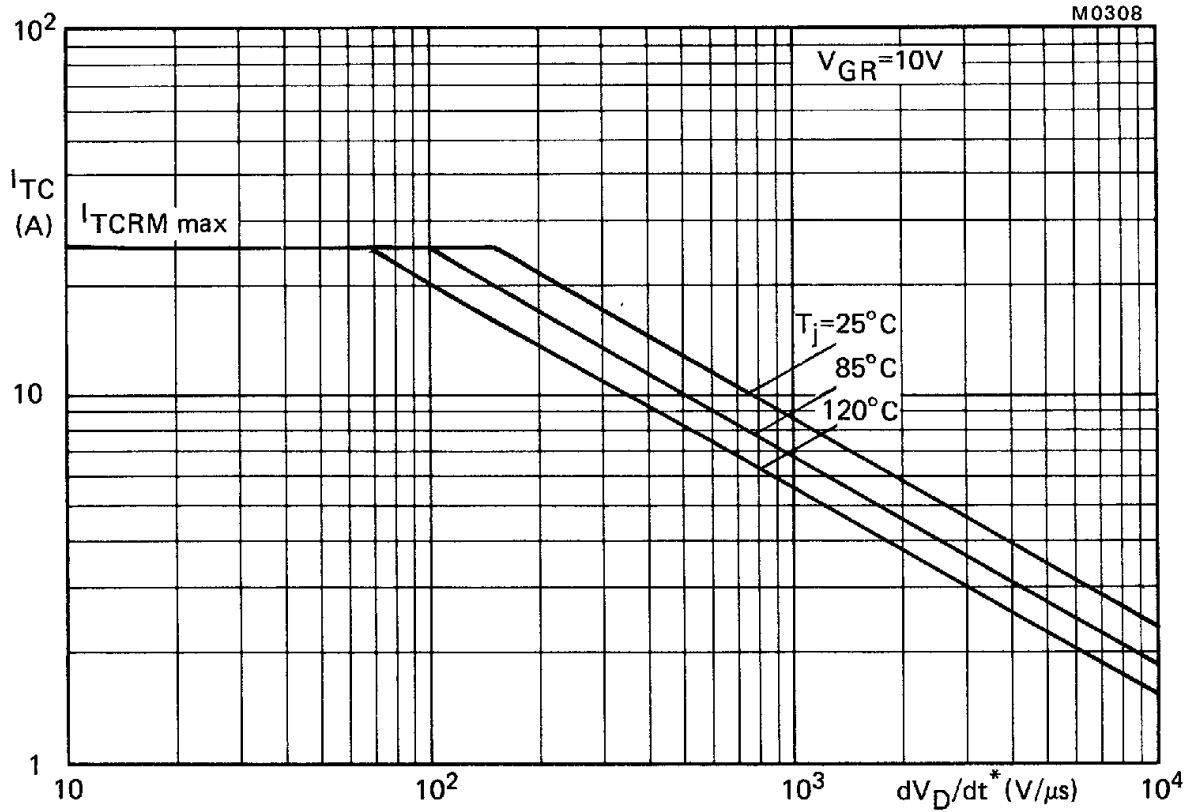


Fig.7 Anode current which can be turned off versus applied dV_D/dt^* ; inductive load; $V_{GR} = 10 V$; $L_G \leq 1.0 \mu H$; $L_S \leq 0.25 \mu H$. * dV_D/dt is calculated from I_T/C_S .

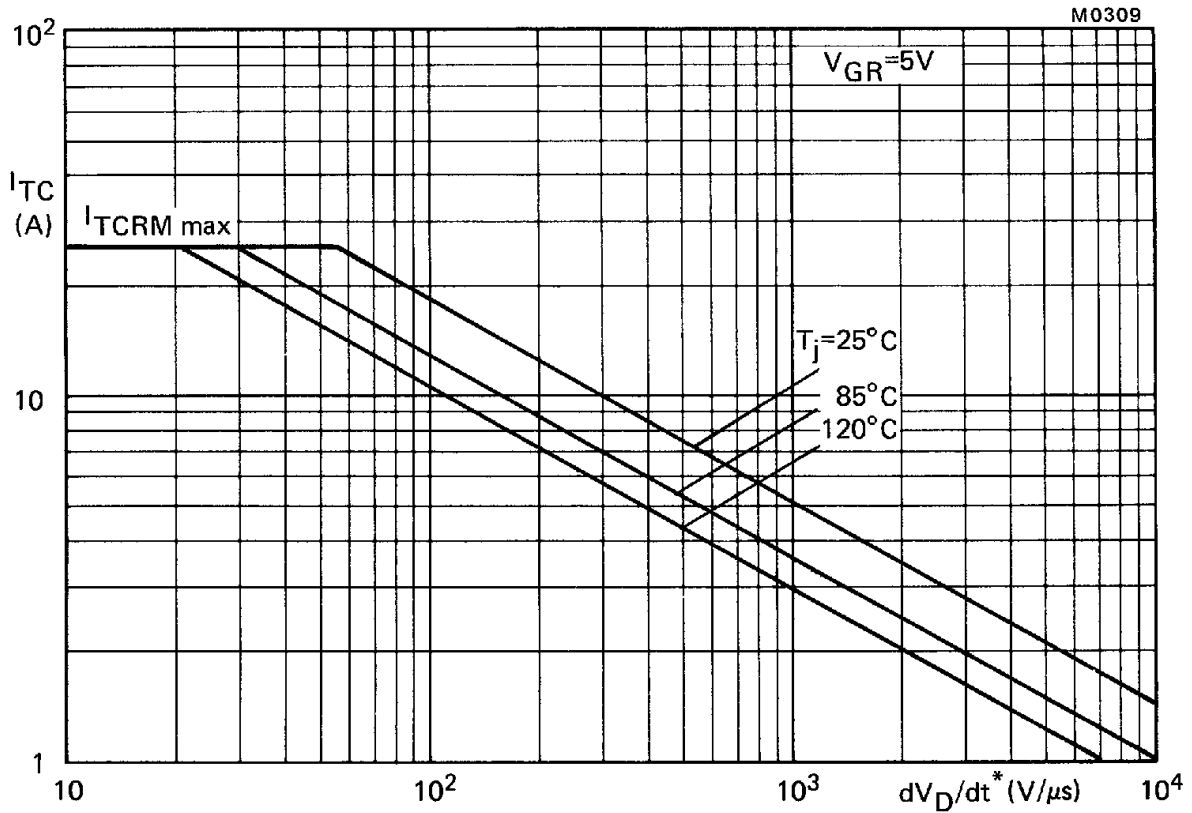


Fig.8 Anode current which can be turned off versus applied dV_D/dt^* ; inductive load; $V_{GR} = 5 V$; $L_G \leq 1.0 \mu H$; $L_S \leq 0.25 \mu H$. * dV_D/dt is calculated from I_T/C_S .

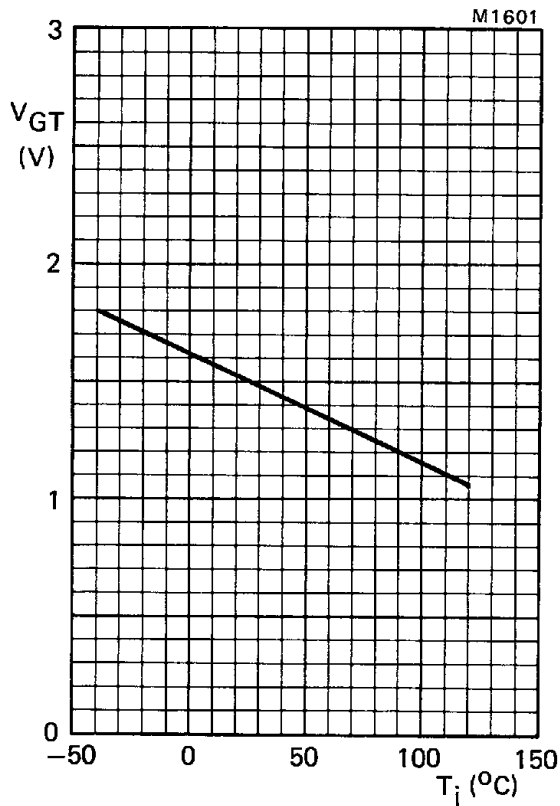


Fig.9 Minimum gate voltage that will trigger all devices as a function of junction temperature; $V_D = 12$ V.

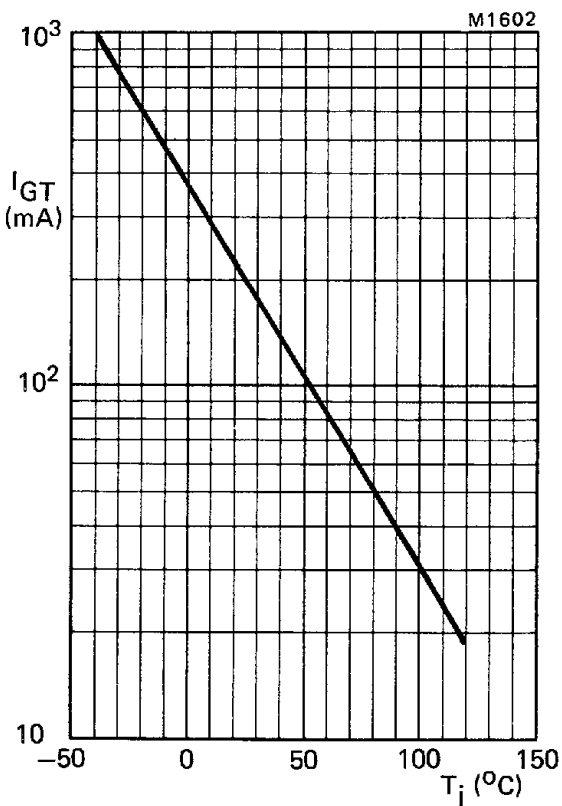


Fig.10 Minimum gate current that will trigger all devices as a function of junction temperature; $V_D = 12$ V.

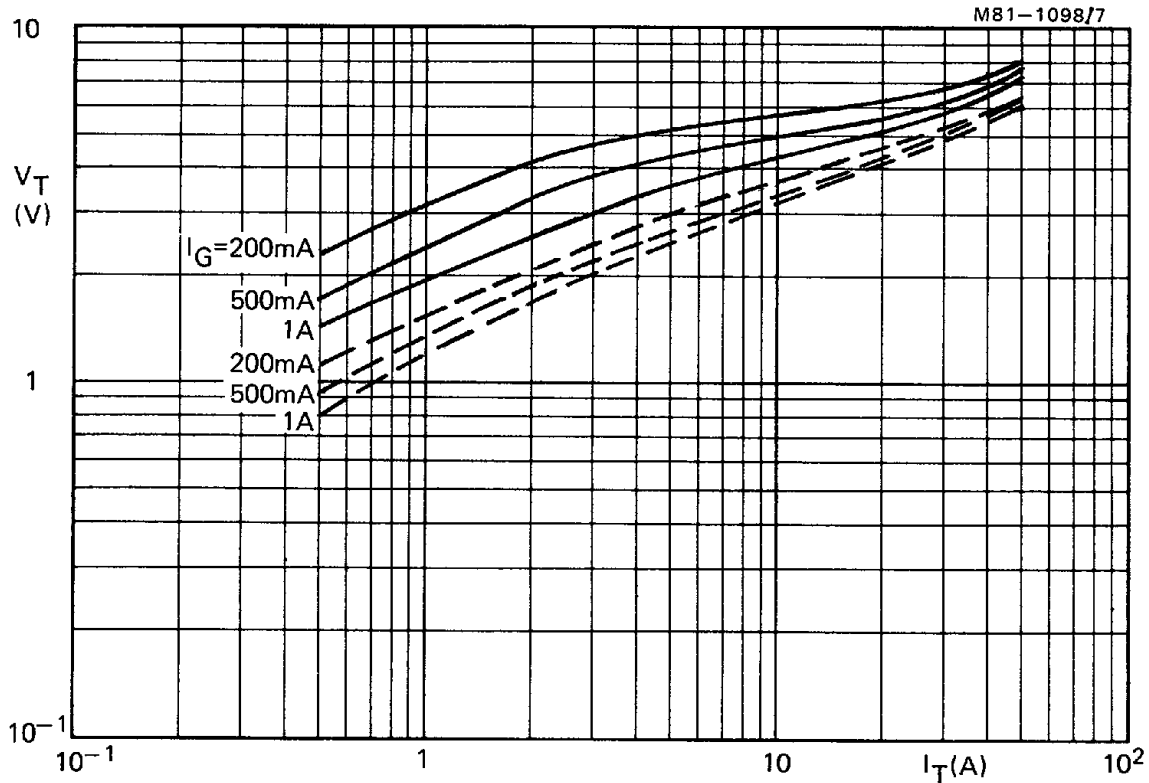


Fig.11 Maximum V_T versus I_T ; — $T_j = 25$ $^{\circ}\text{C}$; - - - $T_j = 120$ $^{\circ}\text{C}$.

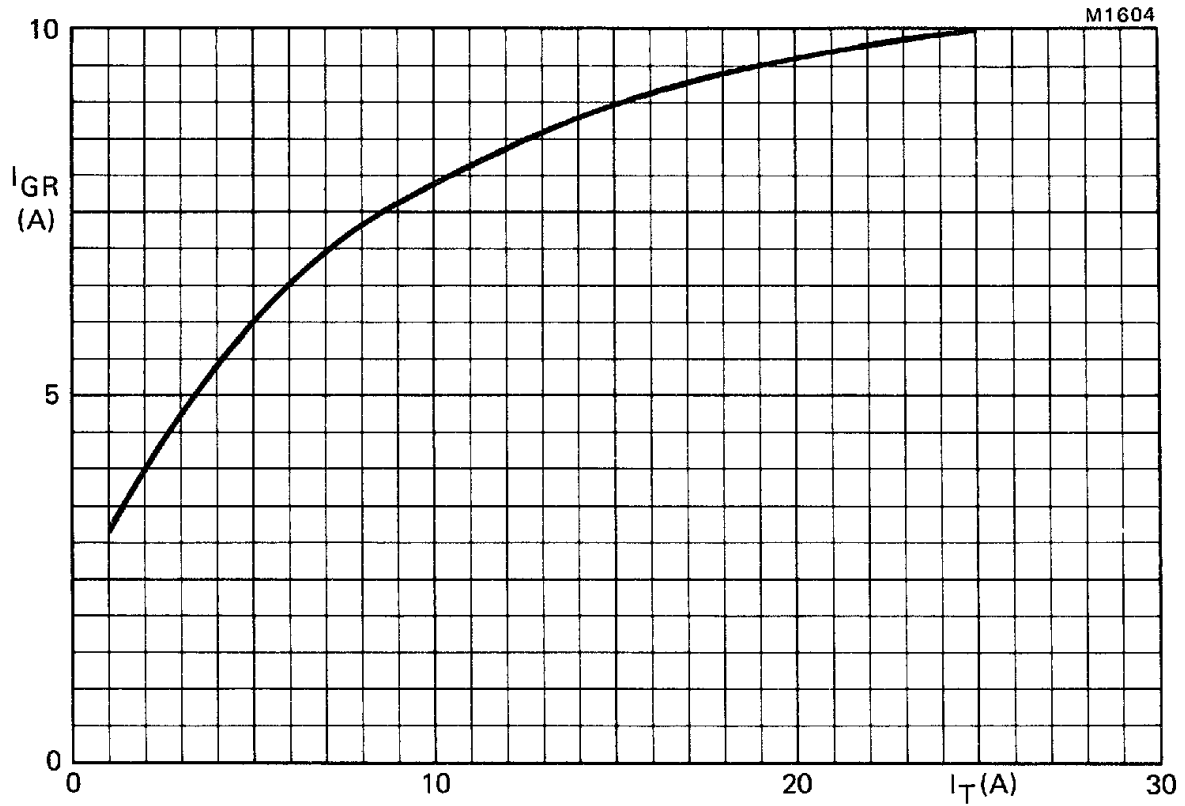


Fig.12 Peak reverse gate current versus anode current at turn-off; inductive load;
 $V_{GR} = 10 \text{ V}$; $I_G = 0.2 \text{ A}$; $L_G = 0.8 \mu\text{H}$; $T_j = 120 \text{ }^\circ\text{C}$; maximum values.

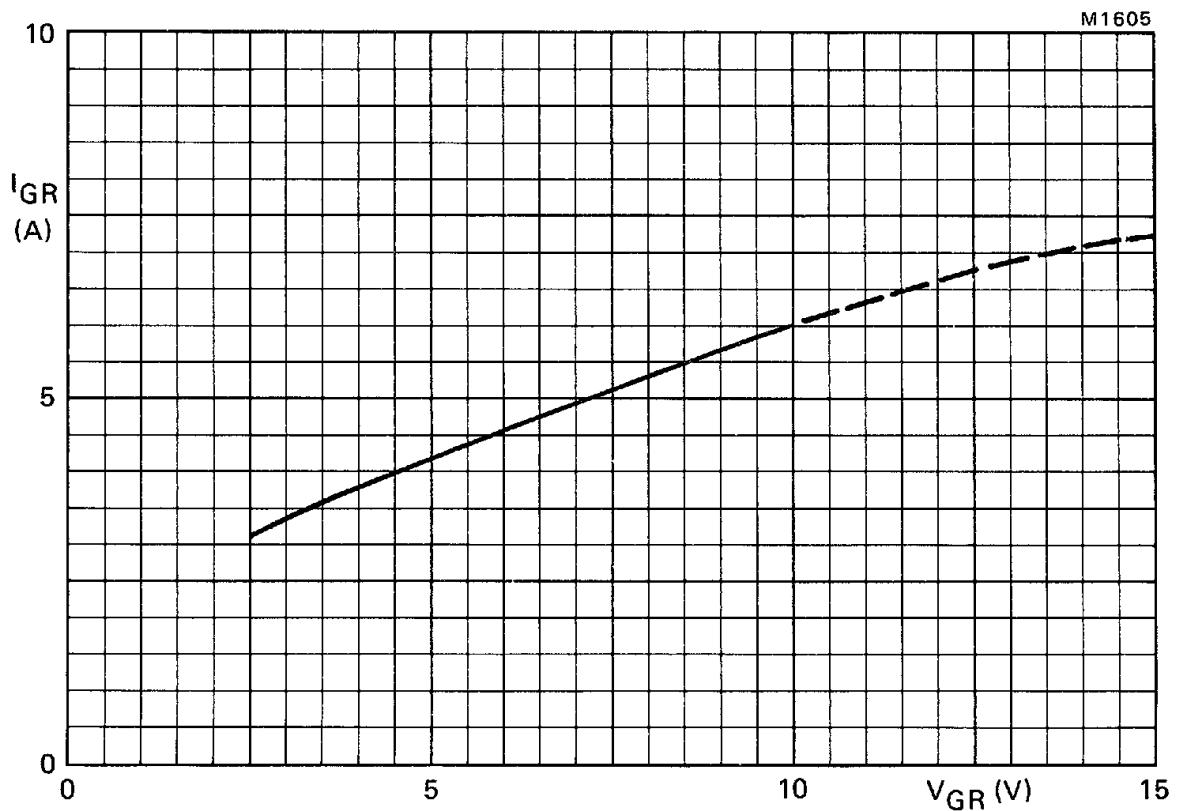


Fig.13 Peak reverse gate current versus applied reverse gate voltage; inductive load; $I_T = 5 \text{ A}$;
 $I_G = 0.2 \text{ A}$; $L_G = 0.8 \mu\text{H}$; $T_j = 120 \text{ }^\circ\text{C}$; maximum values.

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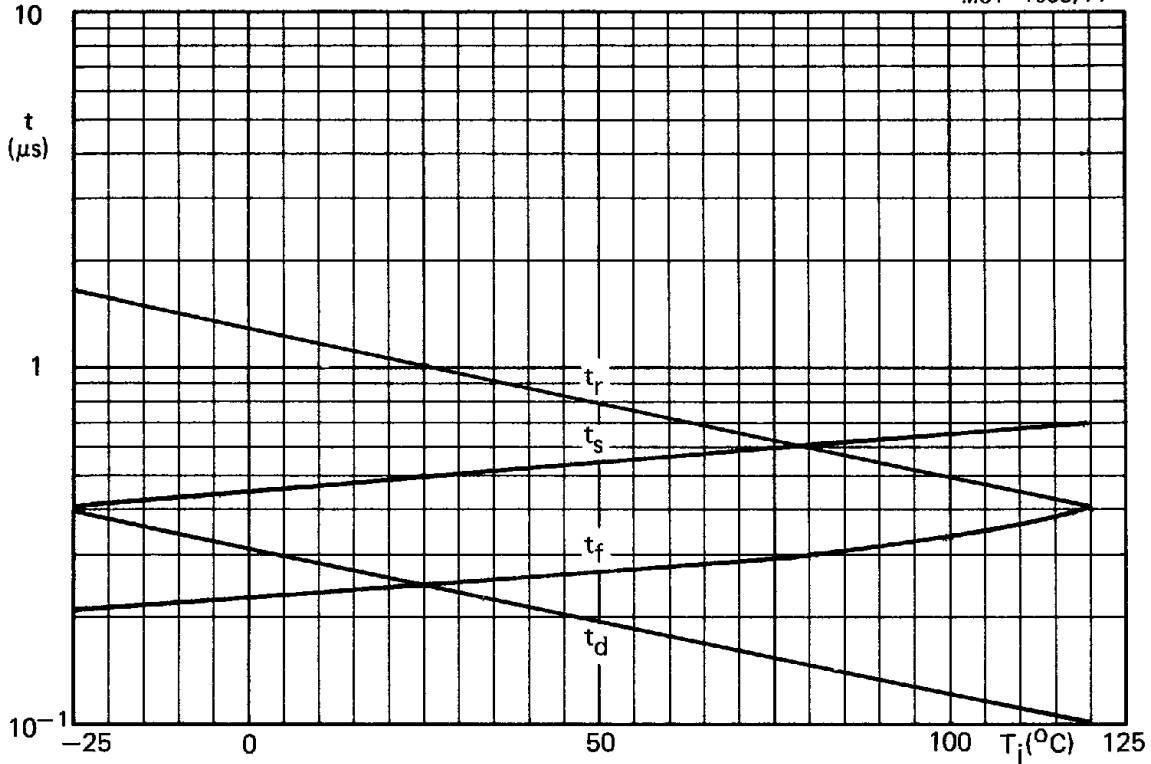


Fig.14 Switching times as a function of junction temperature; $V_D \geq 250$ V; $I_T = 5$ A; $I_{GF} = 0.5$ A; $V_{GR} = 10$ V; $I_G = 0.2$ A; $L_G = 0.8 \mu\text{H}$; maximum values.

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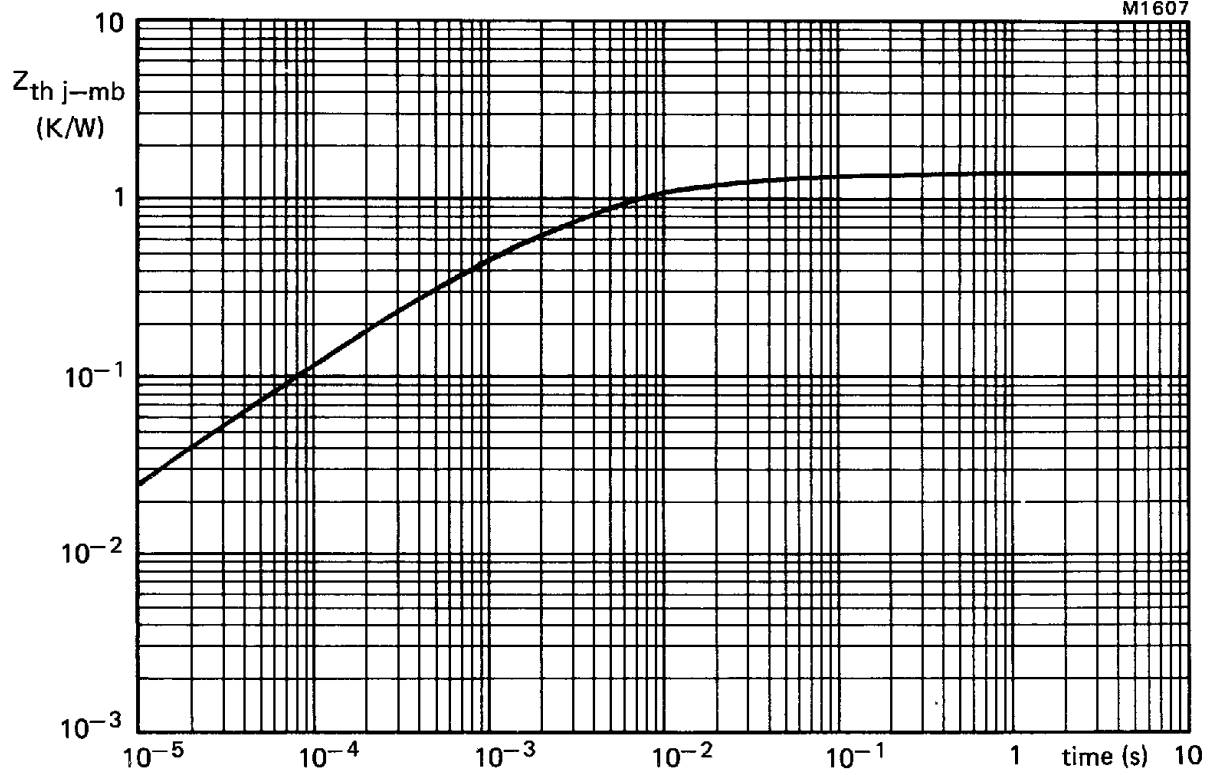


Fig.15 Transient thermal impedance.

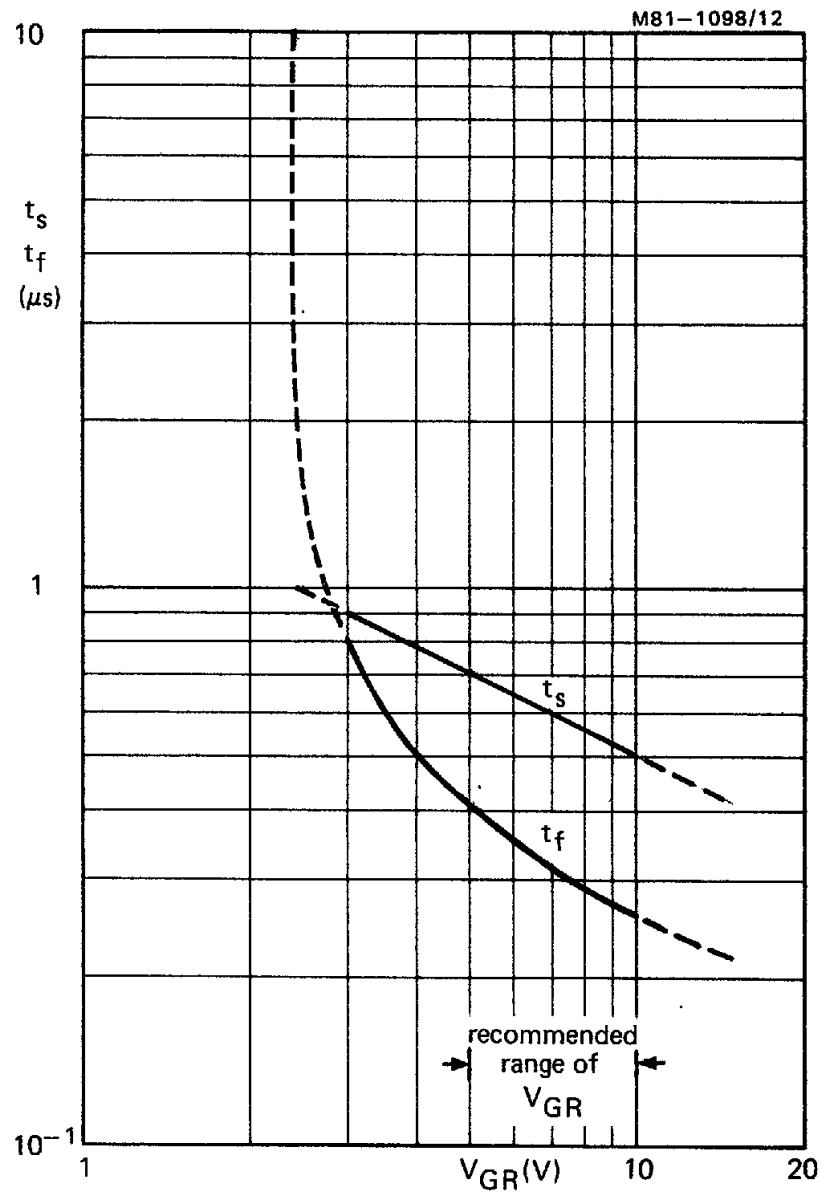


Fig. 16 Storage and fall times versus applied reverse gate voltage; inductive load; $I_T = 5$ A; $I_G = 0.2$ A; $L_G = 0.8 \mu H$; $T_j = 25$ °C; maximum values.

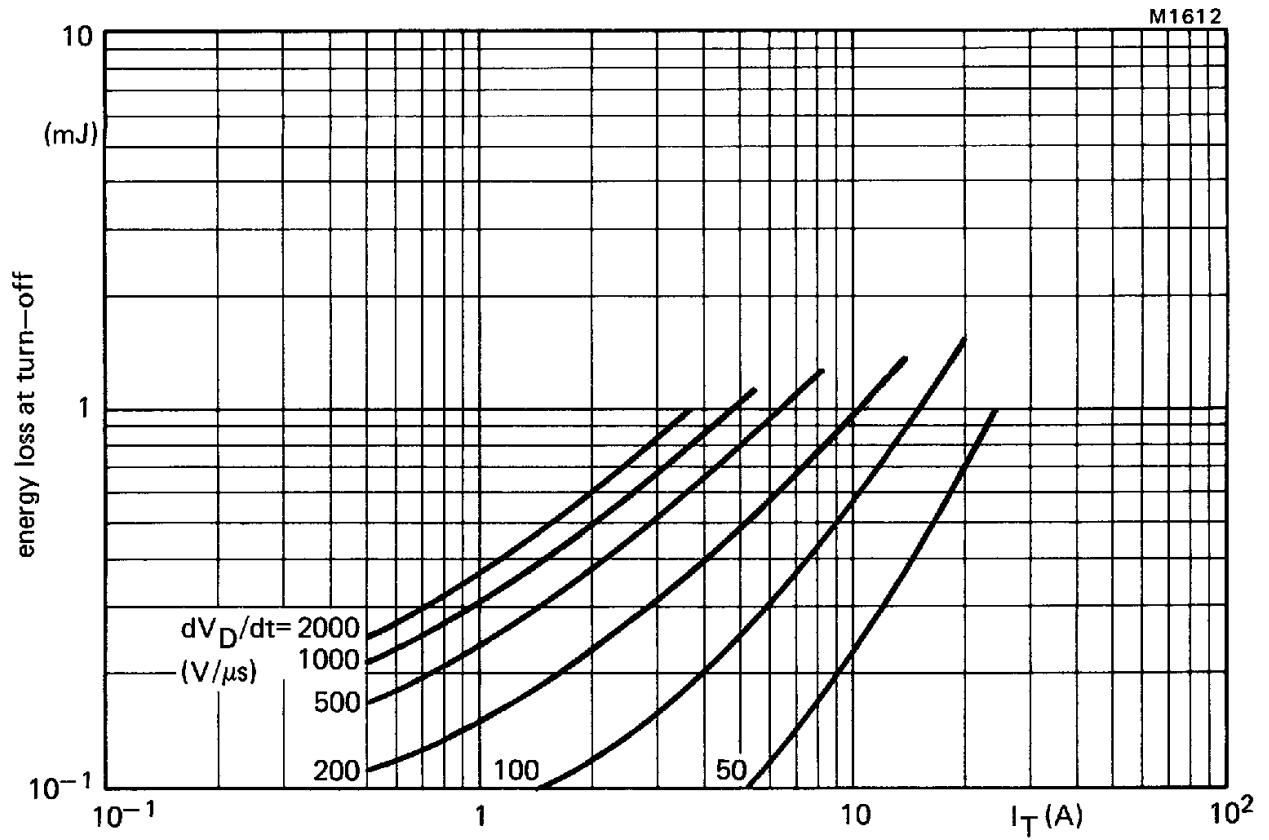


Fig.17 Maximum energy loss at turn-off (per cycle) as a function of anode current and applied dV_D/dt (calculated from I_T/C_S); reapplied voltage sinusoidal up to $V_{DRM} = 1200$ V; $V_{GR} = 10$ V; $I_G = 0.2$ A; $L_G \leq 1.0 \mu H$; $L_S \leq 0.25 \mu H$; $T_j = 120$ °C.

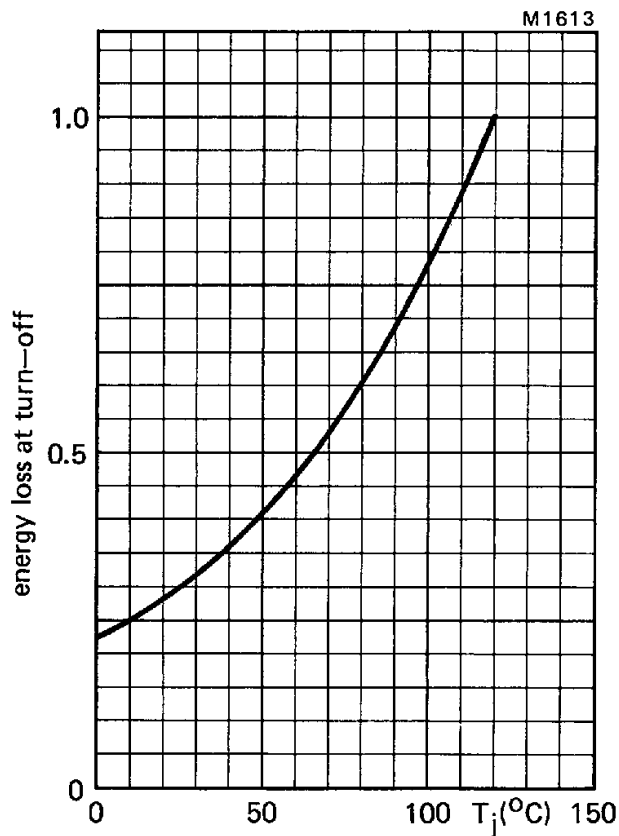


Fig.18 Energy loss at turn off as a function of junction temperature; $I_G = 0.2$ A; $V_{GR} = 10$ V. Normalised to $T_j = 120$ °C.