

GENERAL ALIGNMENT INSTRUCTIONS

NOTE : THIS RECEIVER IS TRANSISTORIZED. SPECIAL CARE MUST BE TAKEN WHEN SERVICING. READ THE FOLLOWING NOTE BEFORE ATTEMPTING ALIGNMENT.

- Alignment requires exact procedures and should be undertaken only when necessary.
- Isolation transformer must be used to prevent shock hazard.
- The test equipment specified or its equivalent is required to perform the alignment properly. Use of equipment which does not meet requirements may result in improper alignment.
- Correct matching of equipment is essential. Failure to use proper matching will result in responses which cannot represent the true operation of the receiver.
- Use of excessive signal from a sweep generator can cause overloading of receiver circuit. Overloading should be avoided to obtain a true response curve. Insertion of markers from the marker generator should not cause distortion of the response.
- The AC Power line voltage should be kept at 230 volts while alignment is carried out.
- Do not attempt to connect or disconnect any wire while the receiver is in operation.
Make sure the power cord is disconnected before replacing any part in the receiver.

TEST EQUIPMENTS

- Digital voltmeter
- Oscilloscope(10:1 probe)
- Direct/Low-capacity probe
- Colour-Bar/Dot/Crosshatch generator
- PIF sweep marker generator (for example, Nihon Tsushinki Model 4723)
- Isolation transformer
- Power supply

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TP3 ACG CONTROL
TP1 TP2 AGC 12V IF INPUT

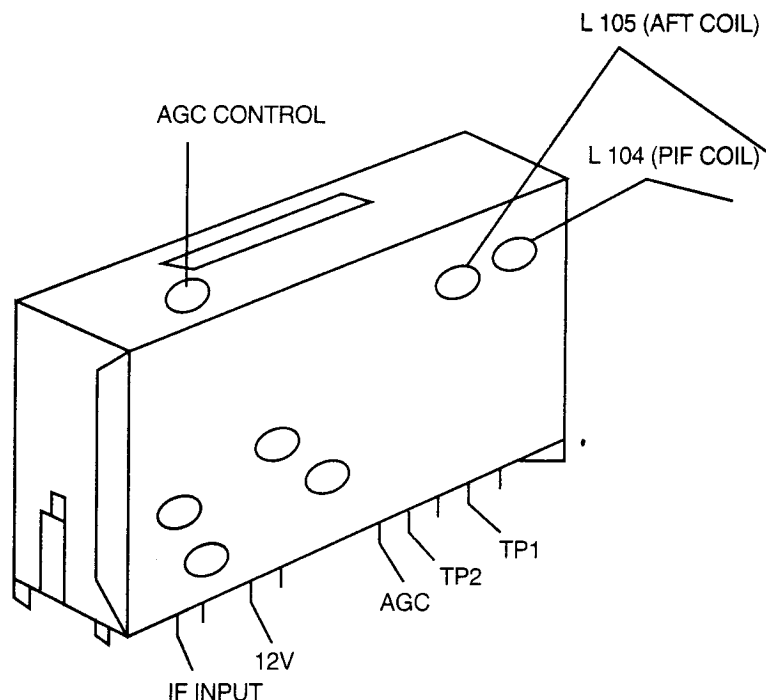


Figure 7-1 IF Module

■ PICTURE IF SWEEP ALIGNMENT AND AFT ALIGNMENT

- Refer to Figure 7, 8 and 9 for alignment points and test equipments connections.

1. Disconnect the IF Module From the Main PCB.

2. PRESET

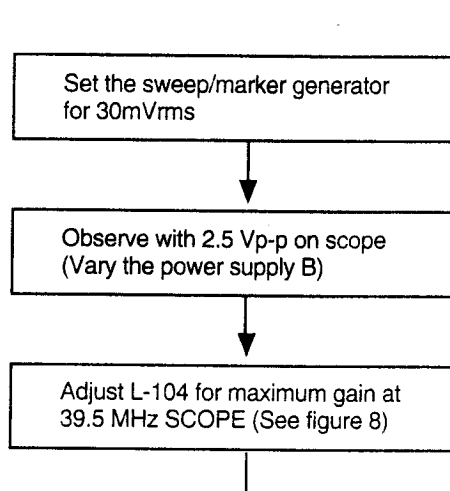
A) Oscilloscope

- Put the scale of X and Y of the oscilloscope to D.C level.
- Put the Mode SW. to CH2.
- Set the horizontal time to X-Y scale.
- Put the horizontal axis (X) to 1V/div. level in order to display all marker freq.
- Put the vertical axis (Y) to 0.5V/div. in PIF adj. and to 2V/div. in AFT adj.

B) PIF SWEEP/MARKER FREQ. SETTING

BAND	31.5	33.5	35.07	37.5	39.5	40.1
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*PIF ADJUSTMENT



* AFT ADJUSTMENT

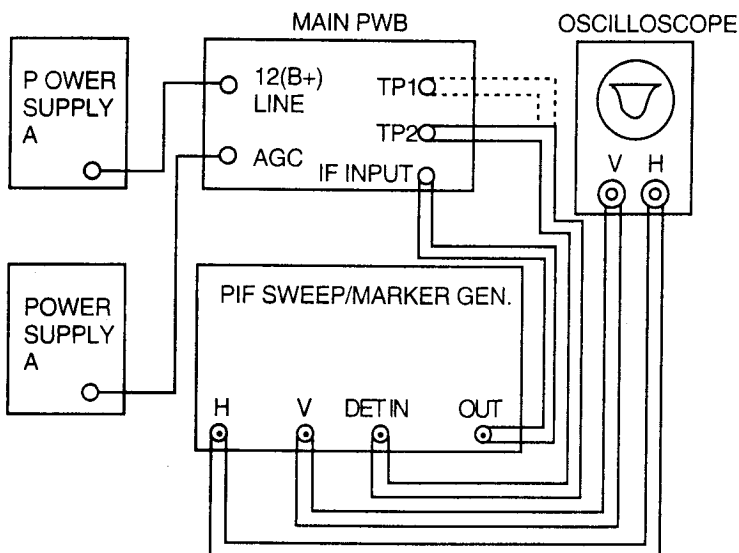
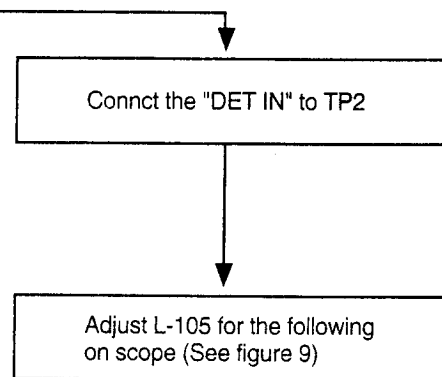


Figure 7-2 Picture I-F Sweep Alignment

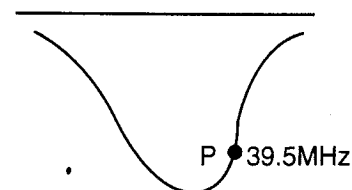


Figure 8 PIF RESPONSE CURVE

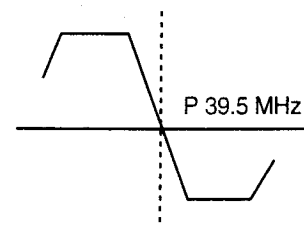


Figure 9 AFT RESPONSE CURVE

*After completing the above steps, disconnect the equipment and adjust the AGC circuit.

■ SOUND ADJUSTMENT

1. ADJ. EQUIPMENT

- 1) Oscilloscope

2. METHOD OF ADJUSTMENT

A) Search the 551.25MHz of PAL-I colour Bar Signal. (Philips Model PM 5518)

B) Adjust the L604 (39.5MHz) coil. (Refer to Fig. 10)

- Test Point : Pin No. 8 of I602 TDA8415
- Adjust this coil to be sine wave without noise.

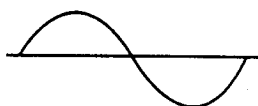


Figure 10 39.5MHz ADJUSTMENT

C) Adjust the Sound 6.0MHz. (Refer to Fig.11)

- Volt/Div 0.2Vp-p, Time/Div 0.2ms (oscilloscope)
- Test Pint : Pin No. 14 of I602 TDA 8415.
- Adjust the L603 coil to be the maximum gain after selecting Mono (1KHz) and then control the sound output to be 1.4Vp-p by using VR602.

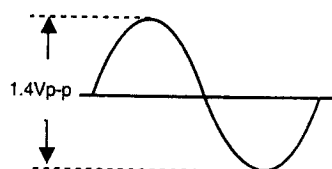


Figure 11 6.0MHz ADJUSTMENT

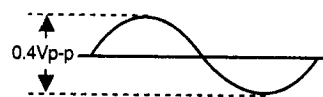


Figure 12 SOUND OUTPUT ADJUSTMENT
(RIGHT, LEFT)

D) Adjust the Sound Right and Left (Refer to Fig. 12)

- Test Pint : Pin No. 3 and 5 of P603. (Volume, Treble and Bass are in maximum state)
- Adjust the sound output to be 0.4Vp-p by varying VR603 (Right).
- Adjust the sound output to be 0.4Vp-p by varying VR 604. (Left)

E) After adjustment as above, please confirm the Mono and Nicam stereo.

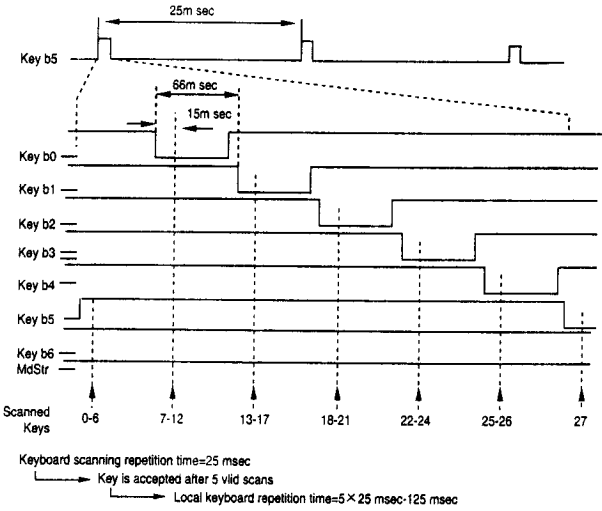
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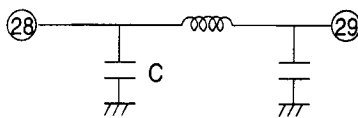
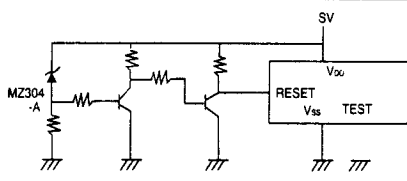
INSTALLATION AND SERVICE ADJUSTMENT

1. PCA84C641

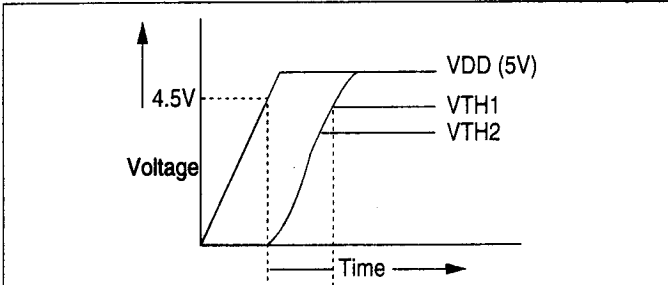
(1). Description of Terminals

Pin No.	Symbol	Name	Function Description												
1	Vt	Tuning Voltage Control Output	<ul style="list-style-type: none">The Vt output is the pulse width modulated output of a 14 bit digital to analog convertor which is split-up in 7 bits for coarse adjustment and another 7 bits for time adjustmentThe basic period of the tuning output signal is $2^{14} \times f_{xtal}/3=4915.2\mu$ sec ($f_{xtal}=10\text{MHz}$).												
2	VOL	Volume Control Output	<ul style="list-style-type: none">Sound volume control output terminal.Output pulse width modulated waveform in 64 levels in accordance with 6-bit latch data (active "H").At the minimum value of VOL, the output waveform becomes "ALL L". After that, whenever the VOL(+) key is pressed, the "H" pulse is incremented by 1. At the maximum value of VOL, the period of "H" becomes 63/64 (duty:63/64)In the following operations, the mute state (minimum value) occurs for a specific time.<ul style="list-style-type: none">(1) Program selection operation.(2) Port output switching.Using the mute key operation, the sound volume output state and mute state can be switched.												
3	BRI	Brightness Control Output	<ul style="list-style-type: none">Outputs the pulse width modulated signal in 64 levels in accordance with 6-bit latch data (active "H"). <div>For Service Manuals Contact MAURITRON TECHNICAL SERVICES 8 Cherry Tree Rd, Chinnor Oxon OX9 4QY Tel:- 01844-351694 Fax:- 01844-352554 Email:- enquiries@mauritron.co.uk</div>												
4	COL	Colour Control Output													
5	CON	Contrast Control Output													
6	BAL	Balance Control Output													
7 8	BNDO BNDI	Band Control Output	<ul style="list-style-type: none">There are control band signal output terminals for a tuner.Assignment for bands is as follows: <table><tr><td>Band</td><td>BNDI</td><td>BNDO</td></tr><tr><td>VHF-L</td><td>L</td><td>L</td></tr><tr><td>VHF-H</td><td>L</td><td>H</td></tr><tr><td>UHF</td><td>H</td><td>L</td></tr></table>	Band	BNDI	BNDO	VHF-L	L	L	VHF-H	L	H	UHF	H	L
Band	BNDI	BNDO													
VHF-L	L	L													
VHF-H	L	H													
UHF	H	L													
9	AFC	Comparison Voltage Input	<ul style="list-style-type: none">Comparison voltage input terminal connected to built-in comparator.Input AFC Signal from TV with level conversion (0 to Vdd).The results of the comparison are used when the autosearch and digital AFT (described later) works.												
10 13 14	AV S-VID AV-1	Scart input S-video input RCA jack input													

Pin No.	Symbol	Name	Function Description
12	AV	TV/VIDEO Selection Output	<ul style="list-style-type: none"> Output pin AV defines whether internal audio/video signals(TV) or external signal from peripheral TV connector are selected. When output state becomes "H", the TV mode is set. When output state becomes "L", the AV mode is set. It always start from the TV mode.
15 16 17 18 19	P000-P06	Local Keyboard Control	<ul style="list-style-type: none"> Input and output pin P00 to P06 are used to scan to local keyboard matrix. The keyboard is scanned every 25m sec; for timing see as follows  <p style="text-align: center;">Fig. 10-1 Local Keyboard Scanning</p> <ul style="list-style-type: none"> If a keypress is detected for 5 periods, it is recognized as valid key command. The repetition of the local keyboard is 125m sec, which is almost equal to the repetition time of the remote control transmitter.
20	MDSTR	System mode Strobe Output	<ul style="list-style-type: none"> This pin is used to scan the various system options. An active low signal is generated at the very first switch-on ("COLD START"). Local keyboard control inputs P00 to P06 are read first; all keys on the local keyboard must be released, otherwise it will wait until they are. The pins that have a diode connection to MDSTR are read back as 0, the pins that do not have such diode connection are read back as a logic 1.
21	GND	GND Terminal	<ul style="list-style-type: none"> Connected to the 0V power supply.
22 23 24 25	R G B BLANK	R.G.B Output Blank Output	<ul style="list-style-type: none"> Outputs R,G and B deliver the colour components for the OSD while output BK is used as a fast blanking signal. The output polarity of the R.G.B and BK terminals are active "H".
26	H.SYNC	Horizontal Synchronous Signal Input	<ul style="list-style-type: none"> Input terminal for CRT display horizontal synchronous signal. Input rectangular pulses whose amplitude is in the range from 0 to 5V. The input polarity is active "H".

Pin No.	Symbol	Name	Function Description
27	V.SYNC	Vertical Synchronous Signal Input	<ul style="list-style-type: none"> Input terminal for CRT Display vertical synchronous signal. Input rectangular pulses whose amplitude is in the range 0 to 5V. The signal state should be active for the time more than that required for three scanning lines. The input polarity is active "H".
28	DOSC OUT	OSD Oscillator Output	<ul style="list-style-type: none"> Input DOSC has to be connected to an external RC network which controls the oscillation frequency of the internal OSD pixel oscillator.  <p style="text-align: center;">Fig. 10-2 The External RC Oscillator</p>
29	DOSC IN	OSD Oscillator Input	
30	TEST	Test Input	<ul style="list-style-type: none"> Input TEST has to be connected to GND.
31	XTAL 1	Microcontroller	<ul style="list-style-type: none"> The XTAL 1 and XTAL 2 are used to control the on-chip oscillator of the μ-controller. XTAL 1 is the input terminal and XTAL-2 the out-put terminal. All internal timing of the μ-controller (except for the OSD part) is derived from this oscillator. The oscillator frequency has to be 10 MHz.
32	XTAL2	Oscillator Control	
33	RESET	Reset Input/Output	<ul style="list-style-type: none"> The circuit shown in figure 10-3 provided to the reset terminal allows the reset function to work when the power is turned ON. In addition, a schmitt circuit is accommodated in reset terminal. The reset state is canceled when the reset terminal voltage "Vdd" exceeds the threshold voltage "VTh1". However once the CPU operation is canceled, unless "V" drops to the threshold voltage "VTh2" the reset function does not work again. In addition to cause the reset function to securely work when the power is turned on its is necessary to set the time to after the power voltage Vdd exceeds 4.5V figure 10-4. When the reset function works, the programme counter in CPU is initialized.  <p style="text-align: center;">Fig. 10-3 System Reset Circuit</p>

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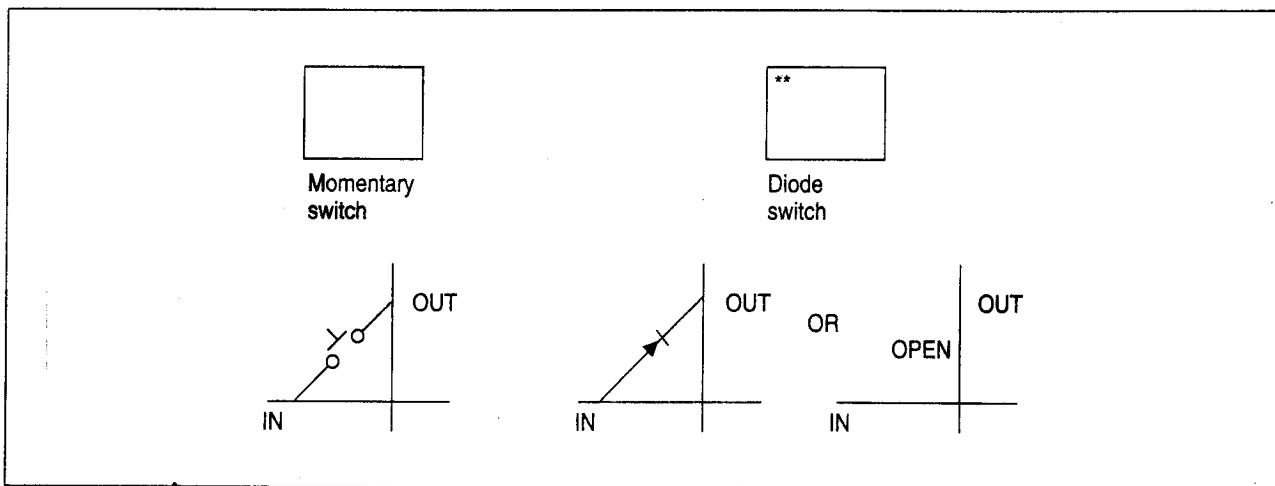
Pin No.	Symbol	Name	Function Description
			 <p>Fig. 104 Relation Between Voltage and Reset Function</p> <ul style="list-style-type: none"> After the reset mode is released, each terminal is set to the initial state and the CPU works from the initial state.
34	IDENT	Video Recognition Input Signal	<ul style="list-style-type: none"> Input terminal of image synchronous signal necessary for auto search and AFT operation. In the case of the determination of the level signal synchronization, the signal state ("H" or "L") which is input at this terminal is determined every 4ms. "H" ... Presence of synchronization "L" ... Absence of synchronization
35	IR	Remote Control Signal Input	<ul style="list-style-type: none"> Remote control signal input terminal.
36	VTR	VTR Time Constant control output	<ul style="list-style-type: none"> This pin controls the VTR time constant of the first PLL in the horizontal synchronization circuit of the TV receiver.
37 38	SYSTEM IN, OUT	System Standard Control Output	<ul style="list-style-type: none"> This pin is used to control the sound and IF part for two different TV transmission standard.
39 40	SCL SDA	I ² C-bus Control Input/Output	<ul style="list-style-type: none"> Pins SCL and SDA are respectively the data and clock wire of the multi-master two-wire bidirection I²C-bus control bus. If a transmission does not succeed the controller will retry it for up to 5 times. If the bus is occupied for longer than 1.18 seconds the μ-controller will generate bursts of nine clock pulses with intervals of 1.18 seconds until bus is free again.
41	POWER	SYSTEM Standby/on Control	<ul style="list-style-type: none"> The switch-mode power supply is controlled. "L" ... Power On "H" ... standby mode
42	Vcc	Power Supply Terminal	<ul style="list-style-type: none"> Connected to the 5V power supply.

(2) Key

A) Key Assignment

	P02(15)	P03(16)	P04(17)	P05(18)	P06(19)
P04(17)		AUTO SEARCH UP			
P05(18)					FINETUNING UP
P06(19)	SELECT		PROGRAM UP	NENU UP	
GND	STORE	CLEAR	MENU DOWN	PROGRAM DOWN	FINE TUNING DOWN
MDSTR (20)		** TUNING TIME	** TUNING TIME		** AFT FOLLOWING

B) Key Type



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2. TA8659AN

(1) Description of Terminals

Pin No.	Symbol	Name	Function Description
1	SCM DEEMP	SECAM de-emphasis	Connect a capacitor to GND for SECAM de-emphasis. #1: B-Y #3: R-Y
2 64	R-Y OUT B-Y OUT	Color differential signal outputs	Load resistor of 8.2k Ω is connected to GND.
4 5	CM DET	SECAM B-Y detector	A 4.250 MHz tuned tank circuit for SECAM B-Y detector is connected.
6	S VCC	VCC for chroma stage	The typical supply voltage is 12.0V BY-pass capacitance is connected to terminal 19.
7	COLOUR	Colour control	Colour saturation increases when the terminal voltage of #7 increase. When the colour killer circuit operates, the terminal voltage of #7 turns to low.
9 8	SRM DET 1 SRM DET 2	SECAM R-Y detector	A 4.406 MHz ytuned tqnk circuit for SECAM R-Y detector is connected.
11 21	SW2 SW3	System logic. I/O	This terminal is an output of system identification logic circuit and also is an input of Manual Select Mode.
12	DL IN	Delayed chroma signal input	1H delayed chroma signal input for PAL/SECAM. The signal phase shift between terminal #14 and terminal #12 should be less than 5 deg. The signal loss of the 1H delay line should be 16dB
13	DC	By-pass	An external capacitor for a bias circuit is connected.
14	DL OUT	Delay line driver output	The PAL/SECAM choma signal output for a 1H delay line. Connect a load resistor of 2k Ω to GND.
15	TINT CONT	Tint control (NTSC Mode)	A phase of burst signal is controlled by this terminal in the NTSC mode.
16	ACC FILTER	ACC filter	An external capacitor ACC filter is connected.
17	DC FEED-BACK	By-pass filter	An external by-pass capacitor for a bias circuit is connected.
18	SECAM IN 50/60	SECAM signal input	SECAM chroma signal is led to this terminal through a Bell filter circuit. Terminal DC voltage is changed by the 50/60 identification logic output. 7.4V for 60Hz 4.4V for 50Hz This identification output is useful for changing a vertical size and shifting a horizontal position on the screen.
19	CHROMA GND	CHROMA GND	GND of the chroma stage.
20	P/N IN VID	PAL/NTSC chroma signal input	PAL/NTSC chroma signal is led to this terminal through band pass filter circuit. The SECAM identification mode is determined by this terminal DC voltage. Open: Line Ident. 15k Ω to GND: Lien+Fram Ident.

Pin No.	Symbol	Name	Function Description
22 23 27	P IDENT S IDENT N IDENT	IDENT filter	#22 PAL ident filter. #23 SCEAM ident filter. #27 NTSC ident filter.
24	S REF	SECAM ident discriminator	A 4.328 MHz tuned tank circuit for SECAM identification is connected. Adjust tank coil so that the recovered DC voltage at terminal 23 is maximum value for 4.328MHz.
25	APC	APC filter	APC filter time constant is connected. When the killer operates, automatic searching circuits operate to widen the pull-in range of the APC circuit. The external time constant also determines the searching speed.
26	4.43 IN	4.43 MHz X'tal IN	4.43MHz X'tal is connected between terminal 26 and terminal 30. No adjustment is required.
28	3.58 IN	3.58 MHz X'tal IN	3.58 MHz X'tal is connected between terminal 28 and terminal 30. During a colour system detection, the X'tals are switched at every 4 APC sweep period. When 3.58 MHz Mode is not needed, 5.6k Ω is connected between terminal 28 to GND.
29	V DRIVE	Vertical output	Output terminal of vertical driver.
30	VCO OUT	X'tal drive	
31	V RAMP	Ramp generator	A vertical sawtooth-wave generator circuit is composed of a ramp capacitor, a zener diode which determines sawtooth starting voltage, and a discharge resistor.
32	V NFB	Vertical NFB	AC and DC negative feedback terminal. The waveform of terminal #32 is equivalent to that of terminal #31 according to the internal operational amplifier.
33	SYNC SEPA	Sync sepa. input	Input terminal of emitter-time constant-type sync separator.
34	GP.TC	Gate Pulse Filter	An external filter for a gate pulse is connected.
35	H BLK	Flyback pulse input, Sync pulse output	Flyback pulse is used as a horizontal blanking of colour differential signal output (#2, #64), colour primary signal output (#41, #42, #43), and 1H delay line output (#14), and also used as a masking pulse for a gate pulse generator, PAL matrix switching, and a SECAM permutator switching. This terminal is also the output of sync signal. During sync period, the terminal voltage of #35 turns to high.
36	AFC F	AFC filter	
37	503 KHz	32 fH VCO	Adjustment-free, 32fH Voltage-Controlled Oscillator. Ceramic resonator is connected. A wide pull-in range covers both 15.625KHz and 15.734KHz of horizontal frequency.

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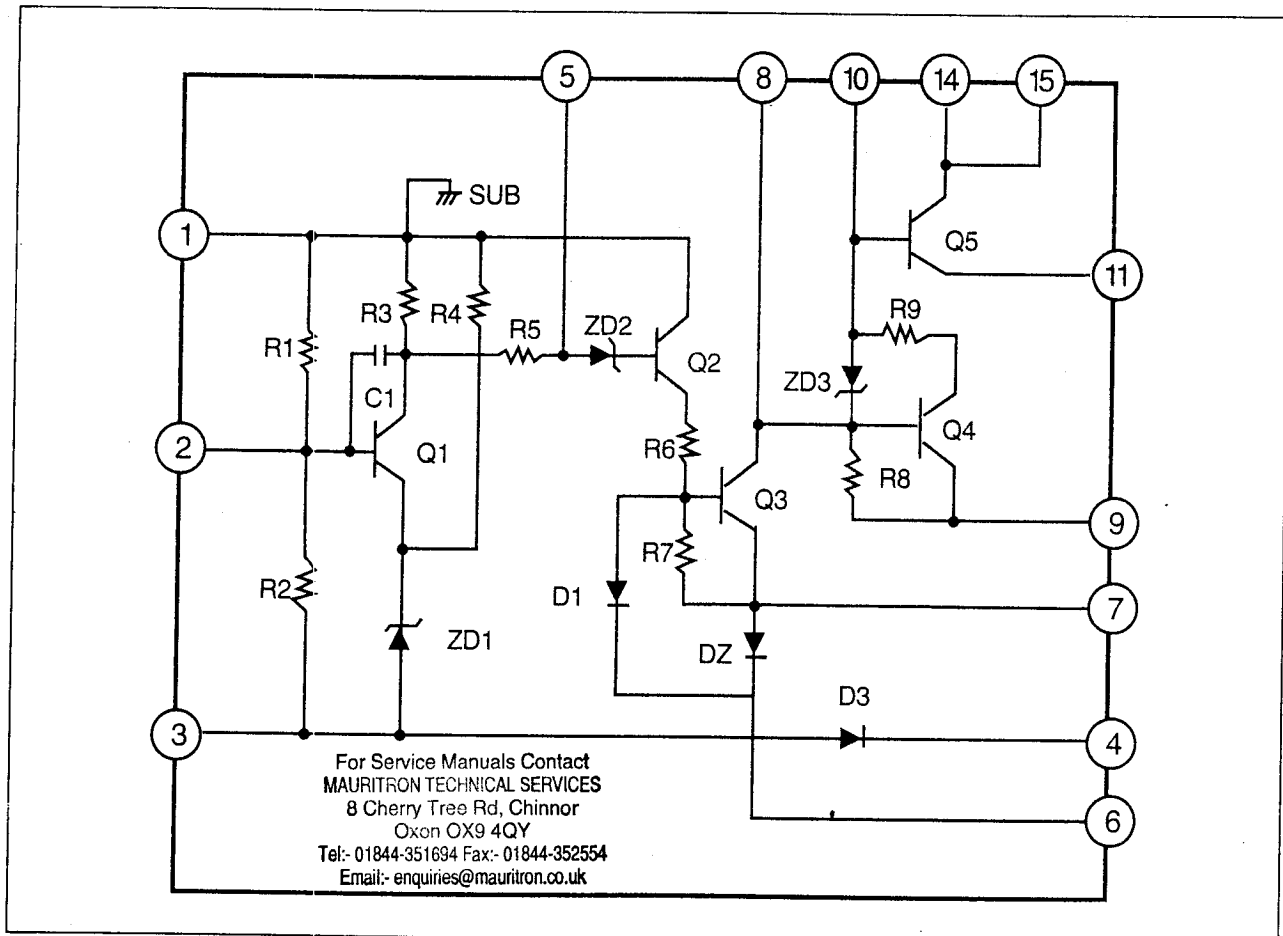
Pin No.	Symbol	Name	Function Description
38	AFC IN	Integrated flyback pulse input	A sawtooth-type horizontal AFC circuit is composed. #38 is an input terminal of integrated flyback pulse (sawtooth). #36 is an AFC filter terminal for 32 fH VCO. A time constant for integration of flyback pulse should be switched so that a screen position is equivalent for 15.734 KHz and 15.625KHz of horizontal frequency.
39	H OUT	Horizontal drive output	An emitter follower output of horizontal predriver. An external load resistor is required.
40	H VCC	H.VCC	Supply terminal for a horizontal deflection circuit. Recommended supply voltage is 9.0V.(9.0V zener diode is required.) A by-pass capacitance is connected to terminal 50.
41 42 43	R OUT G OUT B OUT	R OUT G OUT B OUT	Color primary signal output
44 45 46	R CLAMP G CLAMP B CLAMP	Clamp capacitor	Clamp capacitor for DC restoration is connected.
47 49 51	RTX IN GTX IN BTX IN	R INPUT G INPUT B INPUT	External RGB signal input. An input decoupling capacitor is used as a clamp capacitor. Input signal level is 0.7 Vp-p.
48	BRT	Brightness control	
50	V/D GND	GROUND	GND for video circuit and deflection circuit.
52	X-RAY	X-ray protector	The input terminal of the X-ray protector. #39 Hor. drive terminal turns to low when the input voltage of this terminal exceeds the specified threshold voltage. (1.3K typ.)
53	TV/TV SW	EXT/TV switching signal input	Fast blanking pulse is acceptable. The threshold level is 1.0V typ.
54	HALF TONE	Half-tone/Full-tone switching signal input	When a half-tone circuit is active, the TV video signal amplitude becomes smaller the nominal level. WPS (White peak suppress) switch. This terminal also switched the white peak suppress circuits. When this circuit is active, in case the RGB output voltage becomes higher than 7.5V, the contrast control terminal voltage is lowered by the internal open collector circuit. Time constant is determined by external capacitance and variable resistor value at #59.
55	PICT.CONT.	Picutre sharpness control/mute switch	When #55 voltage becomes lower than 0.7V, the mute function operates. The brightness control circuits become the same condition as when 3V is applied at #48, EXT/TV switch turns to TV mode, and the video signal and the colour differential signal are cut.
56	PICT.IN		Second-order differential video signal input.
57	Y CLAMP	Pedestal clamp	A terminal for a pedestal clamp capacitor.
58	Y IN	Video input	A video signal of sync negative should be applied.

3. STK 73012

- (1) Case Outline: 15pin
- (2) Function: OFF-LINE. Switching Regulator
- (3) Application: Voltage Regulator for Colour TV/VRT use.
- (4) Features: Self-Oscillation type.
- (5) Absolute maximum ratings at TA=25 °C

ITEM	SYMBOL	RATED LEVEL	UNIT
AC input Voltage	V AC	0 TO 280	V RMS
Maximum output power	WO MAX	140	W
Operating ambient temperature	T OP	-10 to +65	°C
Storage ambient temperature	T STG	-30 TO +105	°C
Operating case temperature	TC MAX	105	°C
Thermal resistance	J-C	1.1	°C/W
Junction Temperature	TJ MAX	150	°C

(6) Internal equivalent circuit



4. TDA 2009

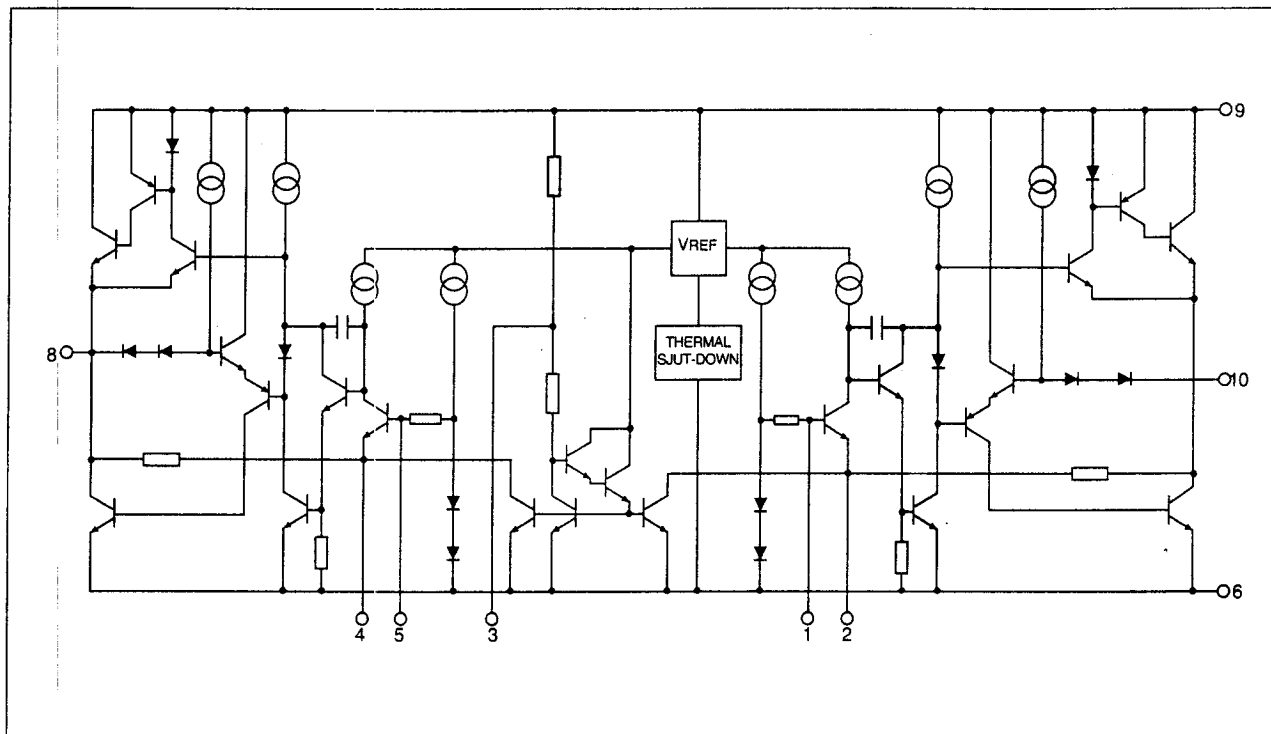
(1) STEREO Amplifier.

The TDA2009 is class AB dual HI-FI Audio power amplifier assembled in Multiwatt package.

(2) Features

- High output power (10W+10W min)
- High current capability (up to 3.5A)
- Thermal over load protection

(3) Block Diagram



(4) Pin Description

PIN NO	DESCRIPTION
1	NON INV. INPUT (1)
2	INV. INPUT (1)
3	SURR
4	INV. INPUT (2)
5	NON INV. INPUT (2)
6	GND
7	N.C
8	OUTPUT (2)
9	+Vs
10	OUTPUT (2)
11	NC

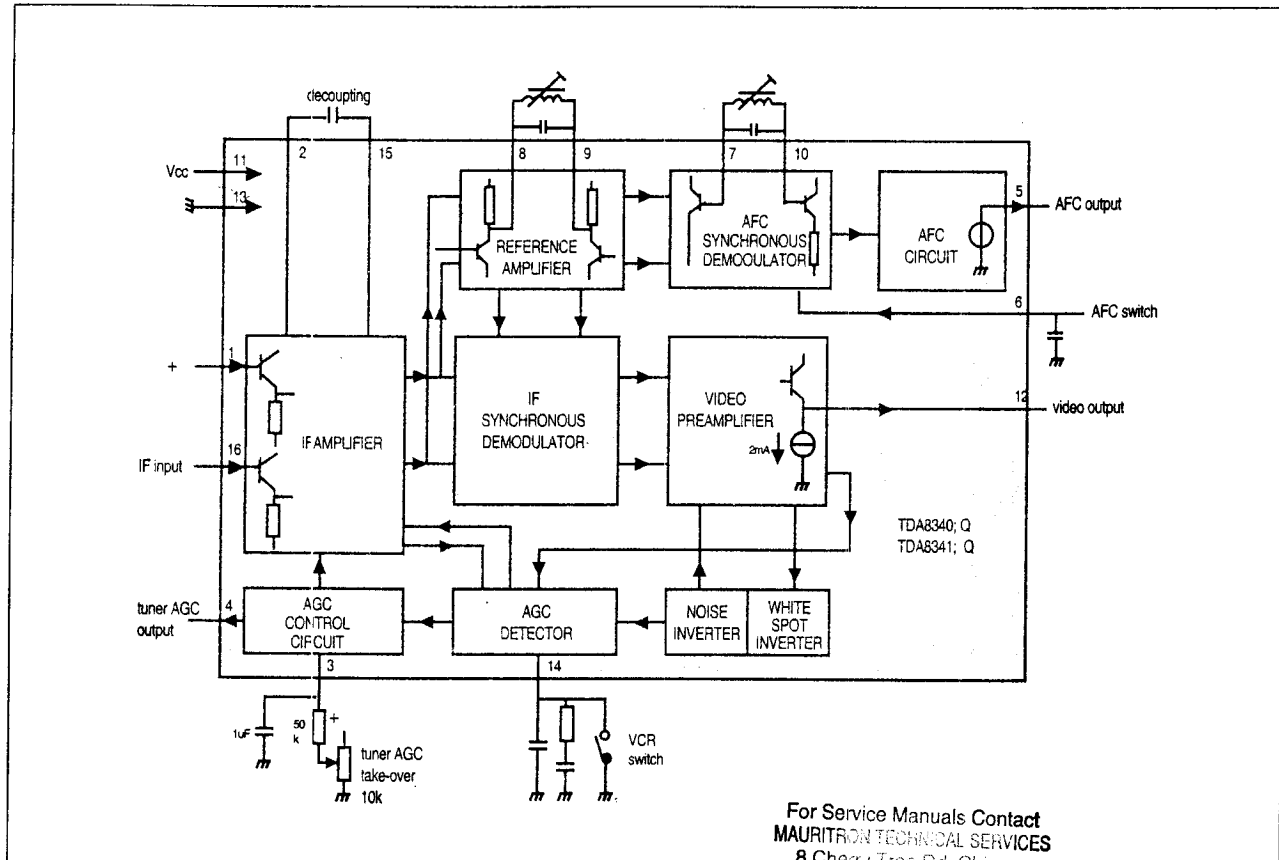
5. TDA 8341

(1) Video and sound IF for TV set function

PIF

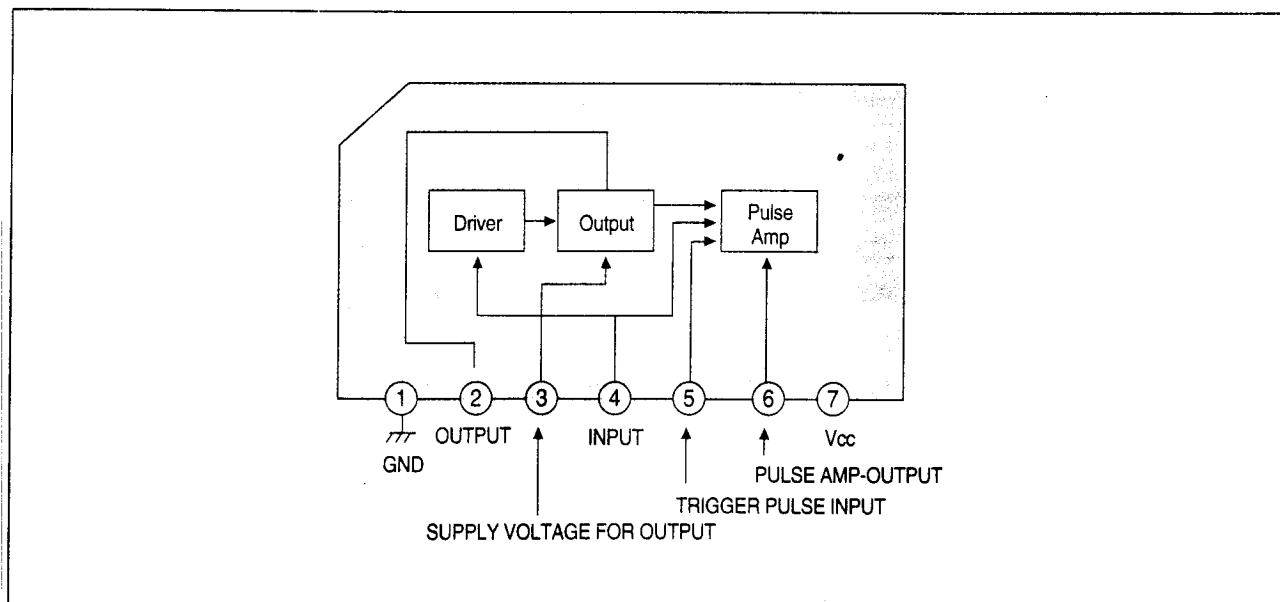
- Fast response AGC (peak) with dual size constants
- Single AFT output with defeat
- Reverse RF AGC
- Black/White noise inverting circuit SIF

(2) Block Diagram



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6. AN5515



7. X24C02P (EEPROM)

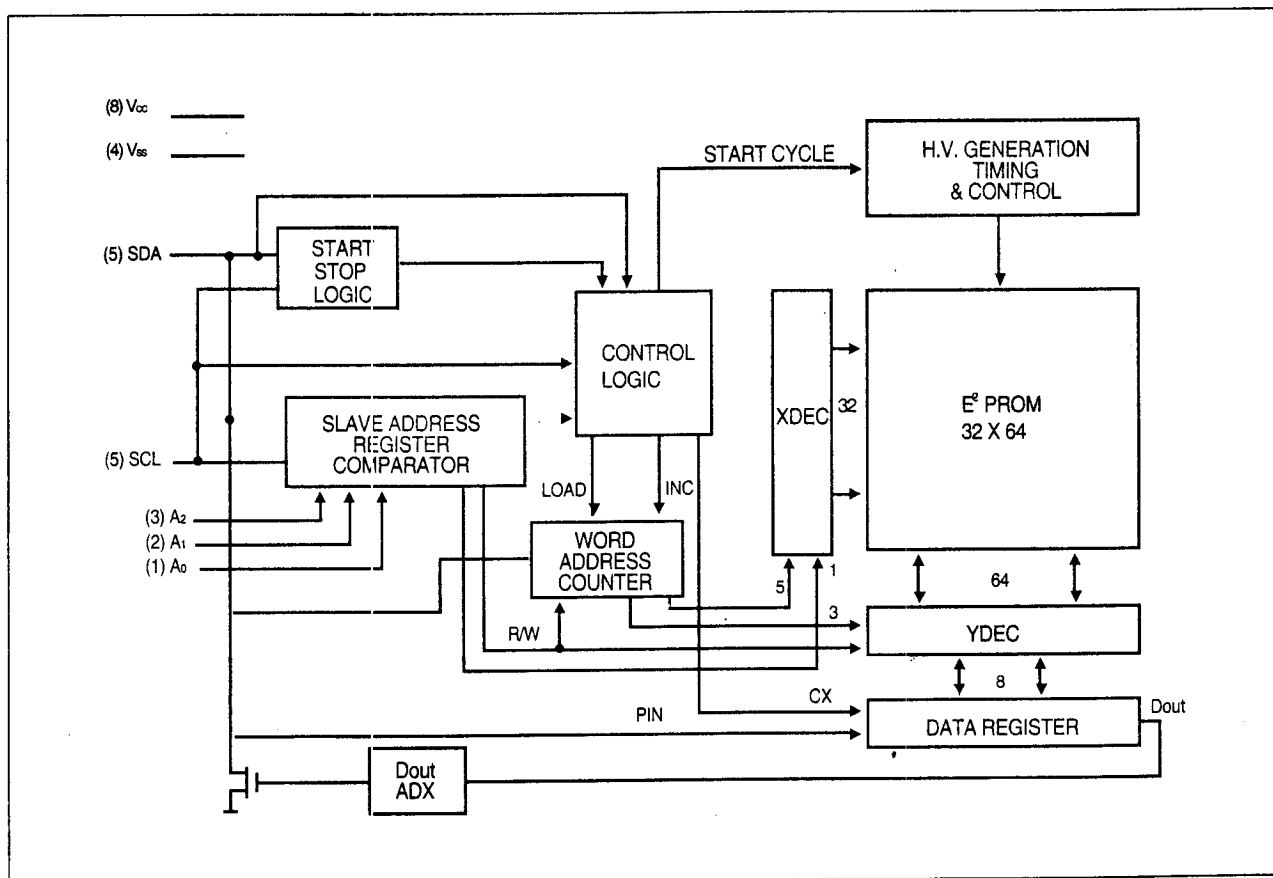
(1) Typical Features

- Low Power CMOS
 - Active Current Less Than 1 mA
 - Standby Current Less Than 50µA
- Internally Organized 256 × 8
- Self Timed Write Cycle
 - Typical Write Cycle Time of 5 ms
- 2 Wire Serial Interface
 - Bidirectional Data Transfer Protocol
- Four Byte Page Write Operation
 - Minimizes Total Write Time Per Byte
- High Reliability
 - Endurance: 100,000 Cycles Per Byte
 - Data Retention: 100 Years
- New Hardwire-Write Control Function

(2) Description

The X24C02 is a 2048 bit serial E²PROM, internally organized as one 256 × 8 page. The X24C02 features a serial interface and software protocol allowing operation on a simple two wire bus.

(3) Block Diagram



(4) Pin Description

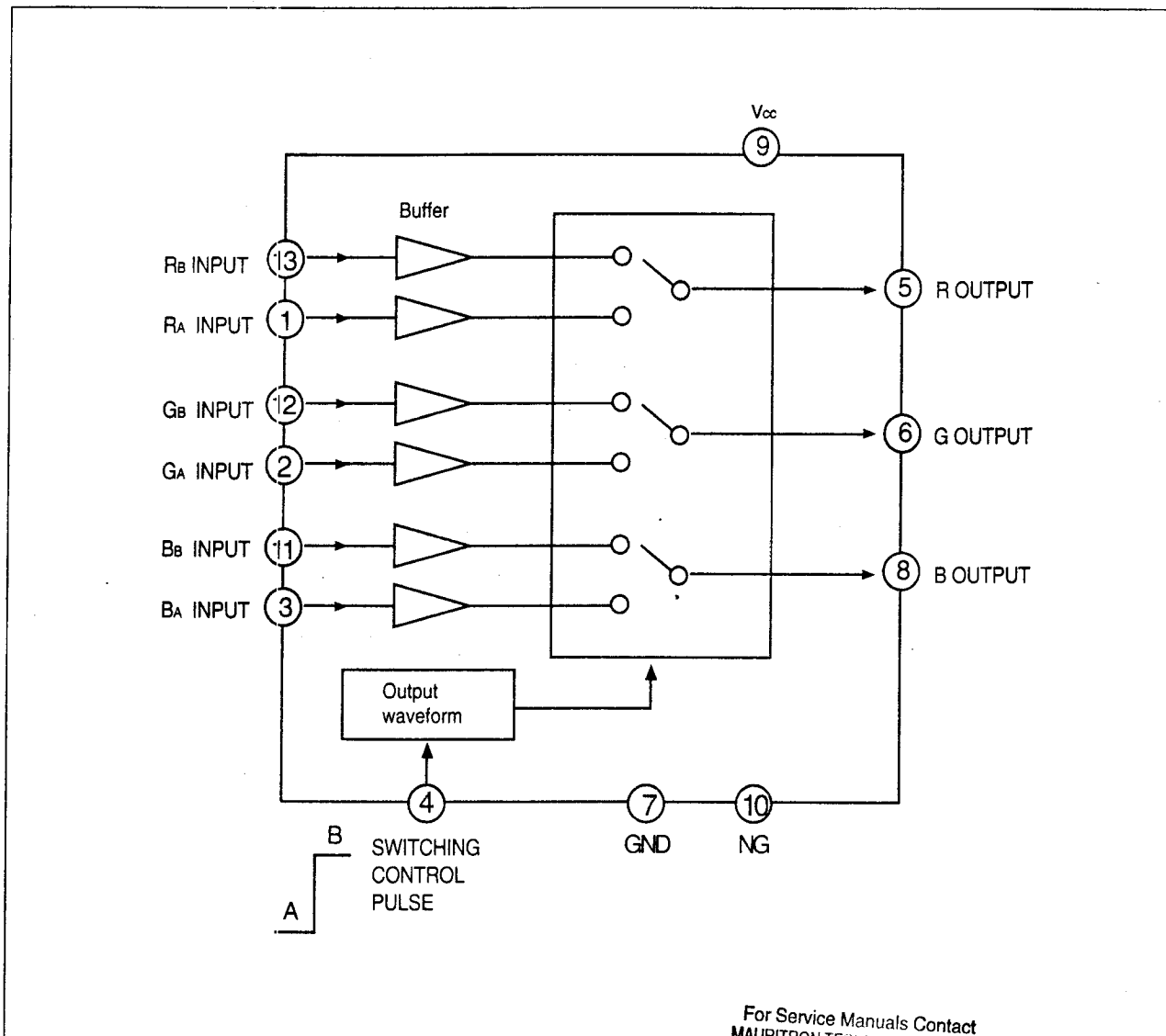
PIN	SYMBOL	FUNCTION
1-3	A ₀ -A ₂	Address Inputs
5	SDA	Serial Data
6	SCL	Serial Clock
7	WC	Write Control
4	V _{SS}	Ground
8	V _{CC}	+5V

8. AN5862K (Analog Switch Circuit for RGB Interface)

(1) Features

- Wide band characteristics
- High data switching speed characteristics

(2) Block Diagram



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(3) Pin Description

Pin No.	Pin Name	Pin No.	Pin Name
1	Ra Input	8	B Output
2	Ga Input	9	Vcc
3	Ba Input	10	NC
4	Switching Pulse Input	11	Bb Input
5	R Output	12	Gb Input
6	G Output	13	Rb Input
7	GND	-	-

9. TEA5114 (RGB Switching Circuit)

(1) Features

- 25 Mhz bandwidth
- Crosstalk: 55 dB
- Short circuit to ground or Vcc protected
- Anti saturation gain changing
- Video switching

(2) Description

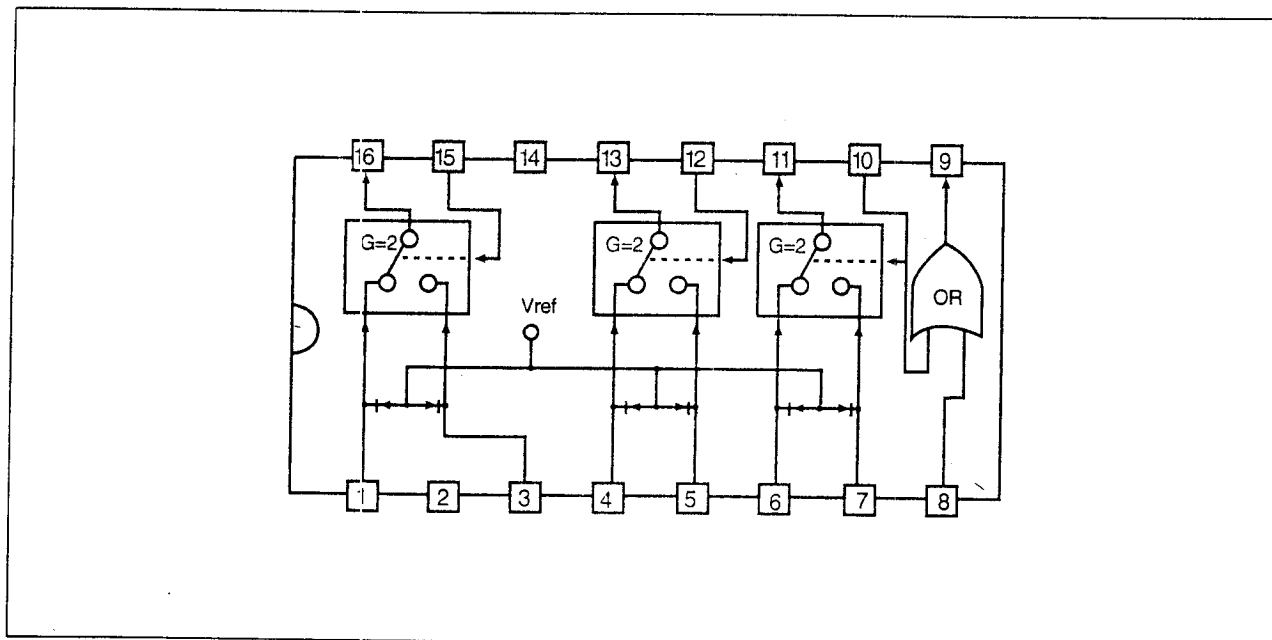
This integrated circuit provides RGB switching allowing connections between peri TV plug, internal RGB generator and video processor in a TV set.

The input signal black level is tied to the same reference voltage on each input in order to have no differential voltage when switching two RGB generators.

An AC output signal higher than 2 Vpp makes gain going slowly down to 0 dB to protect the TV set video amplifier from saturation.

Fast blanking output is logical or between FB1 (Pin 8) and FB2 (Pin 10).

(3) Block Diagram



(4) Pin Description

Pin No.	Pin Name	Pin No.	Pin Name
1	R ₁ Input	9	FB Output
2	GND	10	FB ₂ +FB _B Input
3	R ₂ Input	11	B Output
4	G ₁ Input	12	FB _G Input
5	G ₂ Input	13	G Output
6	B ₁ Input	14	Vcc
7	B ₂ Input	15	FB _R Input
8	FB ₁ Input	16	R Output

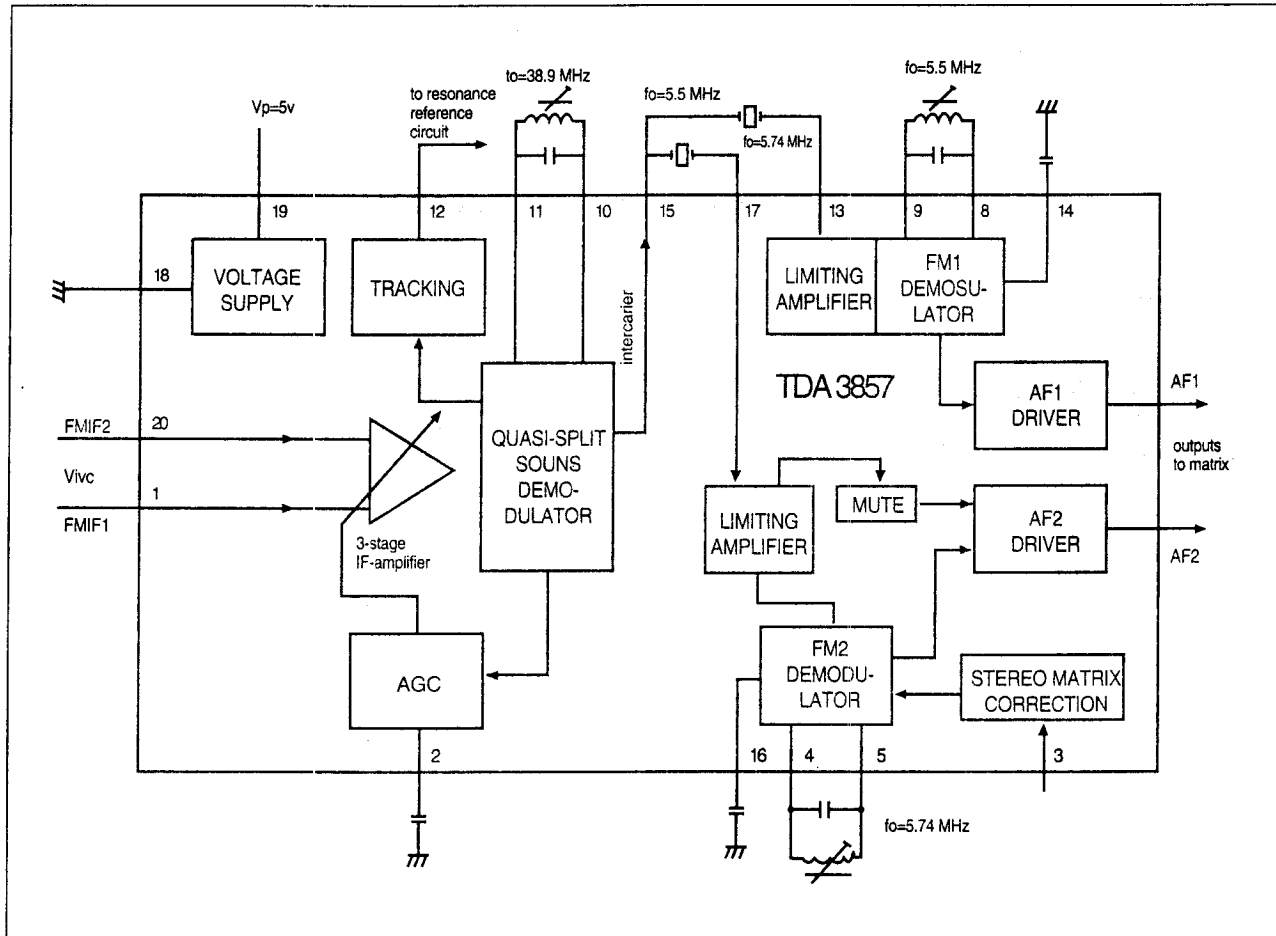
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10. TDA 3857 (FM Sound Demodulator)

(1) Feature

- Quasi-Split sound processor for all FM standards e.g.B/G
- Reducing of spurious video signals by tracking function and AFC for the vision carrier reference circuit
- Automatic muting of the AF2 signal (at B/G) by the input level.

(2) Block Diagram



(3) PIN Description

PIN No	SYMBOL	DESCRIPTION
1	FMIF 1	IF difference input 1 for B/G standard (38.9 MHz)
2	CAGC	Charge capacitor for AM AGC
3	MATR	Input for stereo matrix correction
4	FM2R1	Reference circuit for FM2 (5.74 MHz)
5	FM2R2	Reference circuit for FM2 (5.74MHz)
6	AF2	AF2 output (AF out of 5.74 MHz)
7	AF1	AF1 output (AF out of 5.5 MHz or AM)
8	FM1R1	Reference circuit for FM1 (5.5 MHz)
9	FM1R2	Reference circuit for FM1 (5.5 MHz)
10	VC-R1	Reference circuit for the vision carrier (38.9 MHz)
11	VC-R2	Reference circuit for the vision carrier (38.9 MHz)
12	TRACK	DC: output level for tracking
13	FM11	Inter-carrier input for FM1 (5.5 MHz)
14	CAF1	De-emphasis capacitor for FM1 demodulator (AF1)
15	ICO	Inter-carrier output signal (5.5/5.74 MHz)
16	CAF2	De-emphasis capacitor for FM2 demodulator (AF2)
17	FM21	Inter-carrier input for FM2 (5.74 MHz)
18	GND	Ground (0V)
19	Vp	+5...+8 V supply voltage (pin 28 not connected)
20	FMIF2	IF difference input 2 for B/G standard (38.9 MHz)

11. TDA 8415 (TV and VTR Stereo/Dual sound processor)

(1) General Description

The TDA8415 is a processor of stereo/dual language signals for stereo sound television receivers and VTR, using the switched-capacitor technique.

The AF signals at the TDA8415 inputs must be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L=Left and R=Right)

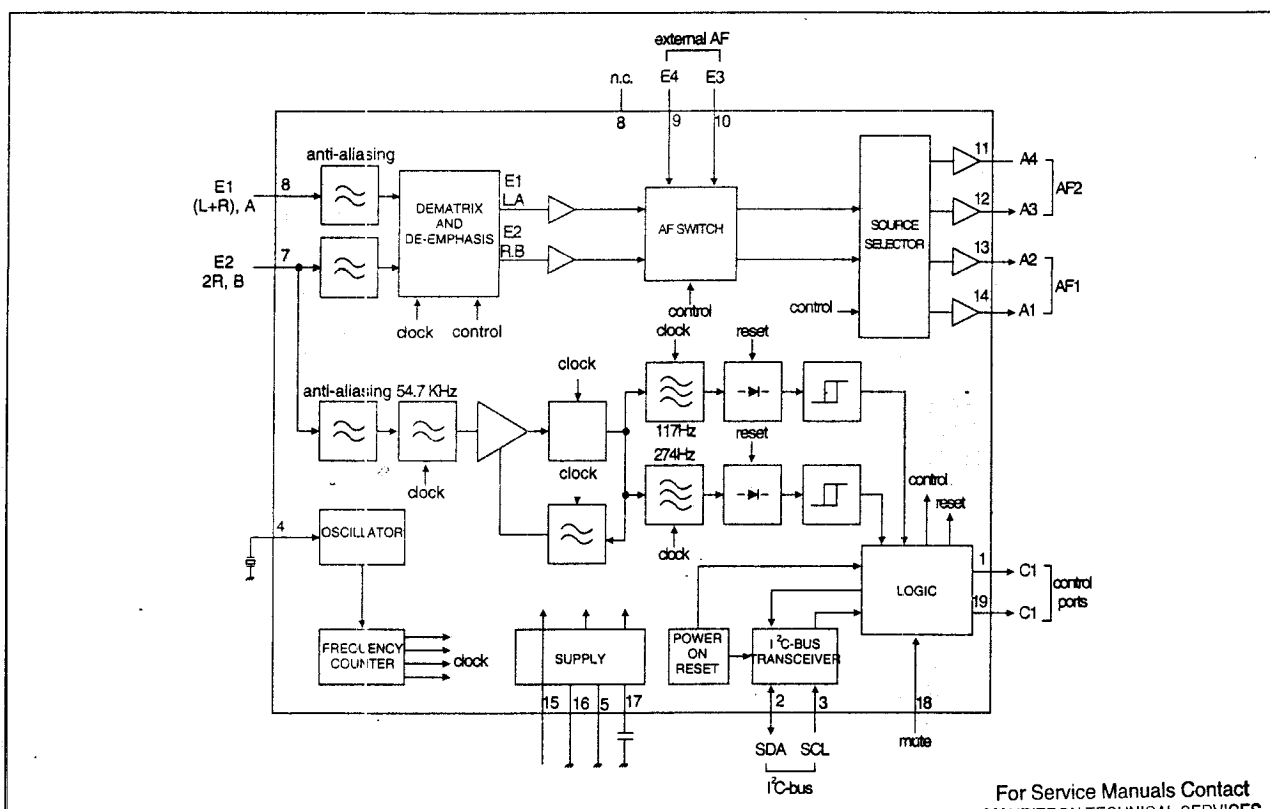
The carrier frequency of the second channel is also modulated by an identification signal (stereo or dual sound).

The device is controlled by a microcomputer via the two line, bidirectional I²C-bus.

(2) Features

- Use of the switched-capacitor technique for signal processing
- Small amount of peripheral components.
- Integrated anti-aliasing filters
- Low distortion AF signal handling
- Integrated de-emphasis with a time constant of 50µs.
- Two general purpose output ports.
- Full ESD protection.

(3) Block Diagram



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(4) Pin Description

Pin No.	Description	Pin No.	Description
1	Control port C1	11	Output A4 AF 2 output
2	SDA, serial data line (I ² C-bus)	12	Output A3 AF 2 output
3	SCL, serial clock line (I ² C-bus)	13	Output A2 AF 1 output
4	Oscillator input (or quartz)	13	Output A1 AF 1 output
5	Digital ground (0 V)	15	Supply voltage Vp
6	Not connected, but reserved	16	Analogue ground (0 V)
7	Sound channel input AF2 (E2)	17	Ripple rejection improvement
8	Sound channel input AF1 (E1)	18	Mute input
9	External AF input (E4)	19	Control port C2
10	External AF input (E3)	20	Not connected, but reserved

12. TDA 8425 (Hi-Fi Stereo Audio Processor)

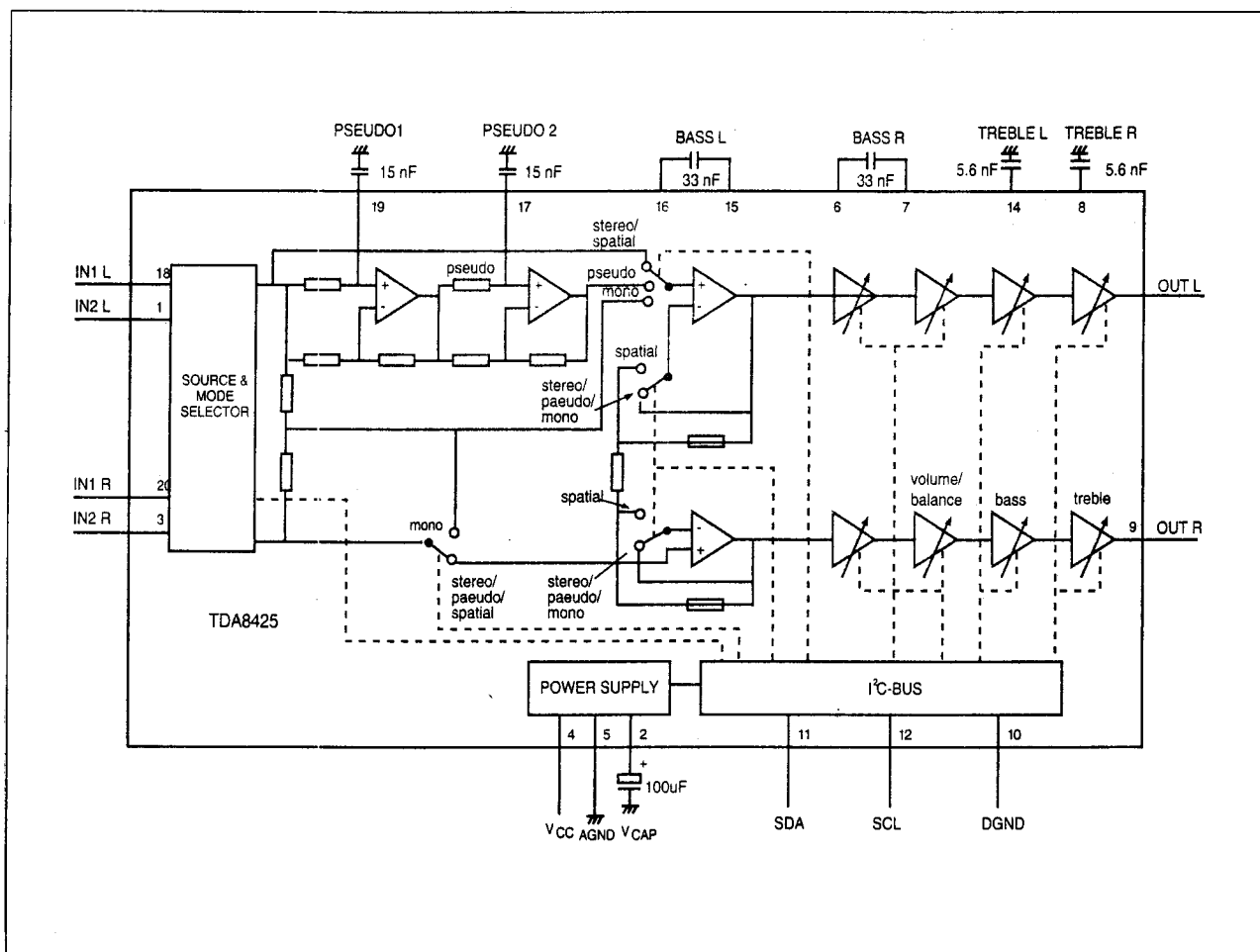
(1) General Description

The TDA 8425 is a monolithic bipolar integrated stereo sound circuit with a loud speaker channel facility, digitally controlled via the I²C-bus for application in hi-fi audio and television sound.

(2) Features

- Source and mode selector for two stereo channels
- Pseudo stereo, spatial stereo, linear stereo and forced mono switch
- Volume and balance control
- Bass, treble and mute control
- Power supply with power-on reset

(3) Block Diagram



(4) Pin Description

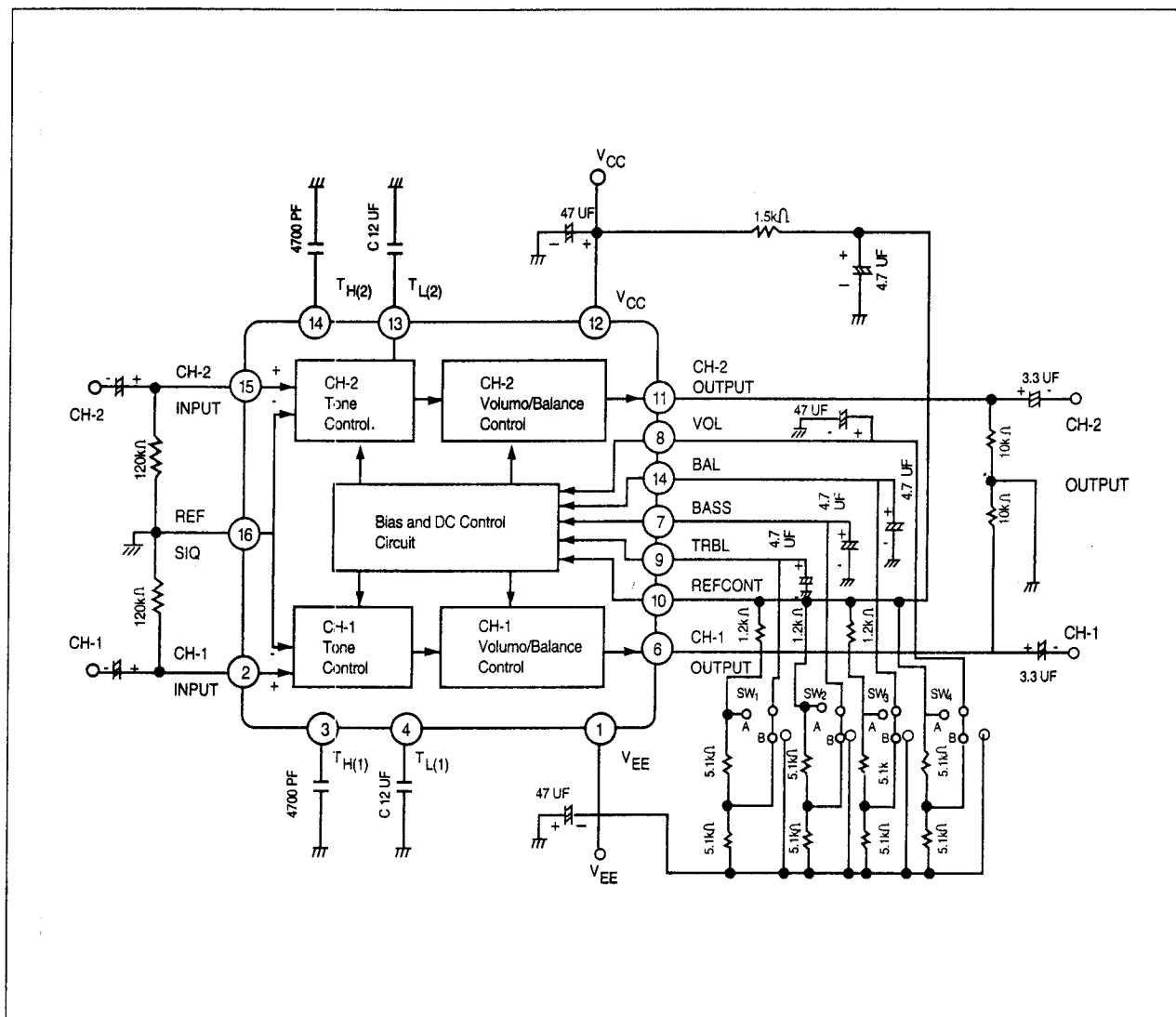
Pin No.	Pin Name	Pin No.	Pin Name
1	1N2 L	11	1N1 R
2	Vcap	12	PSEUDO 1
3	1N2 R	13	1N1 L
4	Vcc	14	PSEUDO 2
5	A GND	15	BASS L
6	BASS R	16	BASS L
7	BASS R	17	TREBLE L
8	TREBLE R	18	OUT L
9	OUT R	19	SCL
10	D GND	20	SDA

13. TDA 7630P (Dual, Volume/Balance/Tone (Bass/Treble) DC Control IC)

(1) Features

- Dc controlled dual volume, balance, tone (bass, treble) IC
- Suitable for TV multiplex sound receiver and remote controlled applications.

(2) Block Diagram



(3) Pin-Description

Pin No.	Symbol	Description	Pin. No.	Symbol	Description
1	VEE	Negative Power Supply	9	BASS	Bass Control
2	INPUT-1	Input Channel-1	10	TRBL	Treble Control
3	TH(1)	Treble turning frequency setting.	11	OUTPUT-2	Output channel-2
4	TL(1)	Bass turning frequency setting.	12	VCC	Power supply
5	REF CONT	Reference control	13	TL(2)	Bass turning frequency setting
6	OUTPUT-1	Output channel-1	14	TH(2)	Treble turning frequency setting
7	BAL	Balance control	15	INPUT-2	Input channel-2
8	VOL	Volume control	16	REF SIG	Reference signal

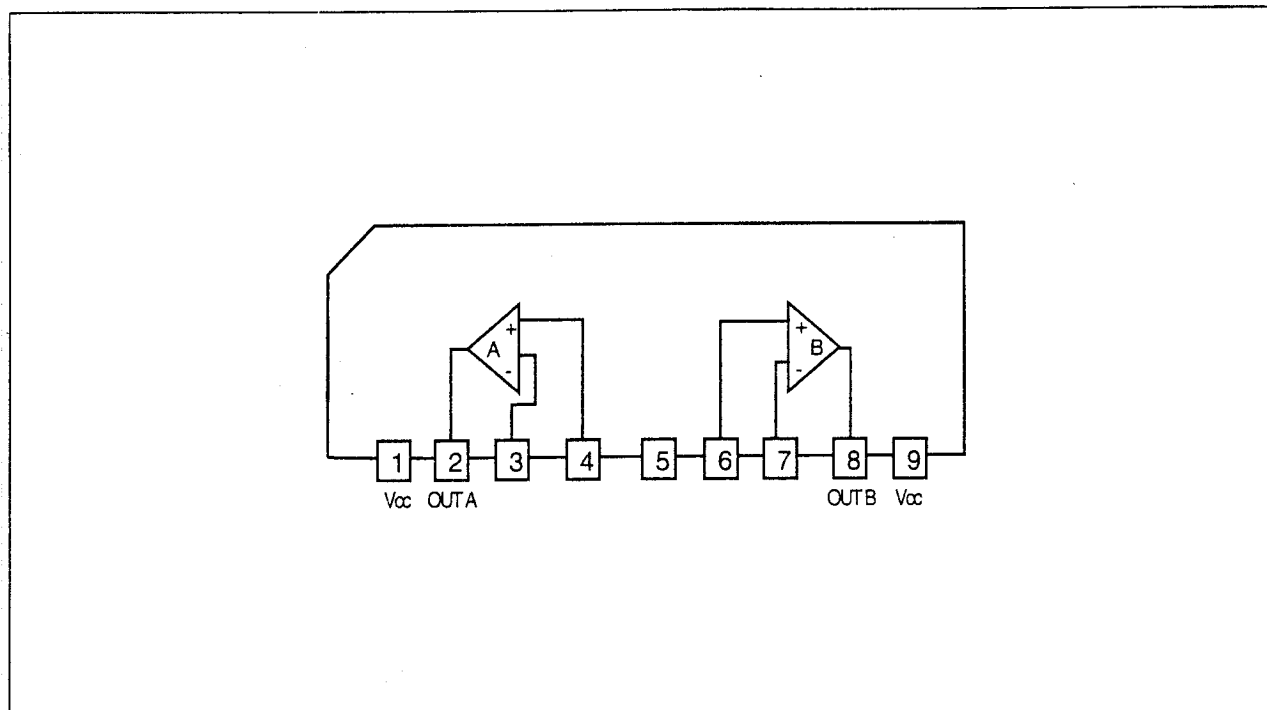
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14. KIA 6259S (Audio Amplifier)

(1) Feature

- Low noise dual pre-amplifier for general audio

(2) Block Diagram



(3) Pin Description

Pin No.	Pin Name
1	Vcc
2	OUT A
3	IN (-) A
4	IN (+) A
5	GND
6	IN (+) B
7	IN (-) B
8	OUT B
9	Vcc

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15. SAA 7280 (Terrestrial Digital Sound Decoder)

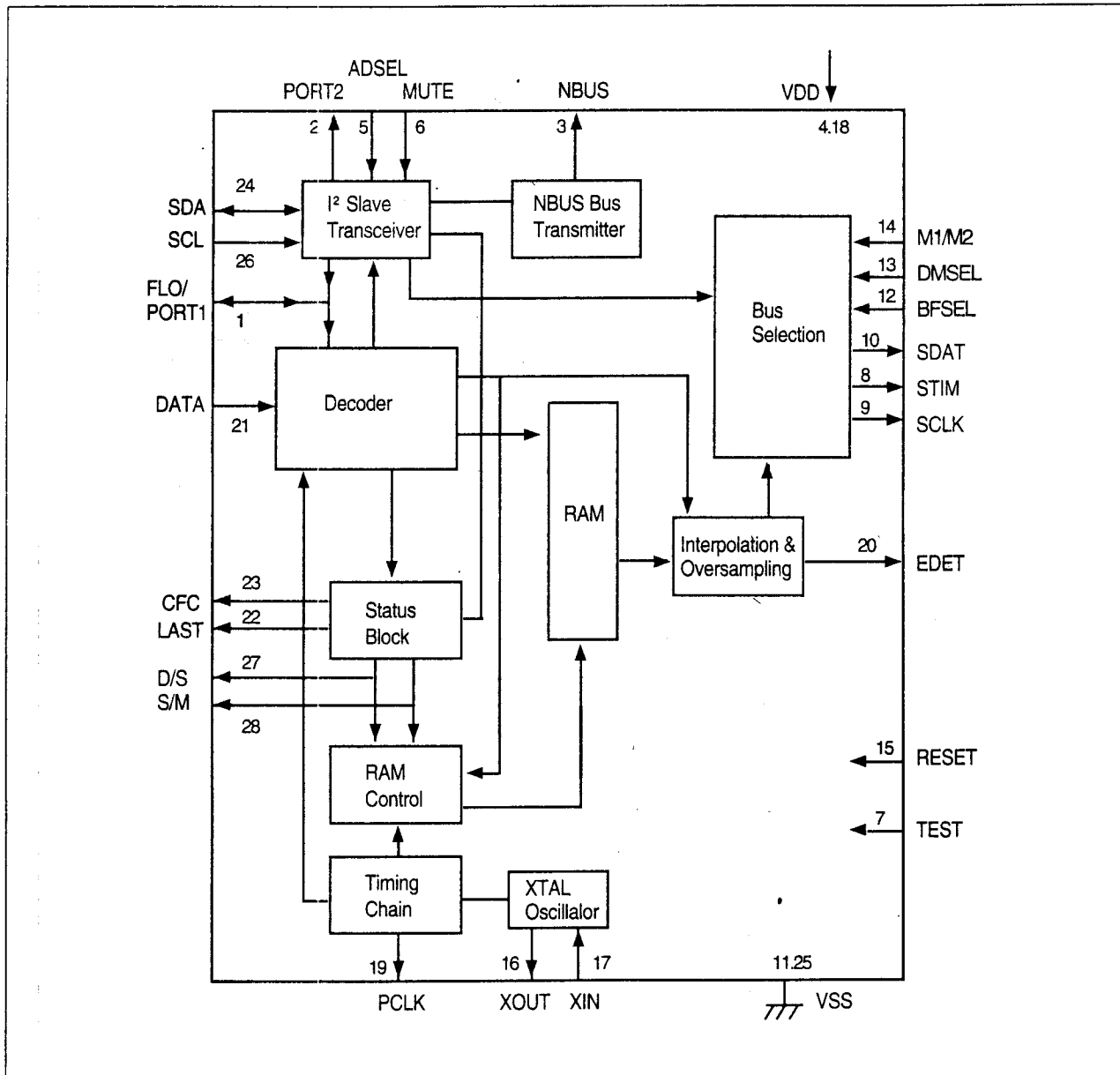
(1) General Description

- The SAA 7280 is a CMOS integrated circuit that performs all the digital decoding functions for the NICAM 728 digital stereo sound system.

(2) Features

- Full EBU NICAM 728 specification decoder
- Microcomputer controlled by I²C
- Automatic decoding and output configuration depending upon transmission
- Three-State outputs for sound bus

(3) Block Diagram



1. Pin Description

Pin No.	Pin Name	Description of Function																											
1	FLO/PORT1	This I/O is a reserve sound switching flag over-ride signal when selected as an input, which is used in the logical equation for the 'LAST' output. It defaults to an input, but can be set via I ² C control. When selected as an output by the PT1EN bit in the I ² C control register, it becomes a port output pin controlled by bit PORT1 via the I ² C control register.																											
2	PORT2	Output pin providing a port out controlled by bit PORT2 via the I ² C control register. See fig 2.																											
3	NBUS	This intermittent data line contains control information. It is used to transfer specific information sent via the I ² C bus on sub-address 0. It has a unique start condition followed by a fixed amount of data sent with separator bits to avoid duplicating the start condition.																											
4,18	VDD	+5 volt power supplies.																											
5	ADSEL	The I ² C slave address select input allows selection of one of two separate slave addresses. <div style="display: flex; justify-content: space-around;"><div>ADSEL</div><div>TDSO Slave Address</div></div> <table style="margin-left: auto; margin-right: auto;"><tr><th></th><th>A6</th><th>A5</th><th>A4</th><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>R/W</th></tr><tr><td>High</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>X</td></tr><tr><td>Low</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>X</td></tr></table>		A6	A5	A4	A3	A2	A1	A0	R/W	High	1	0	1	1	0	1	1	X	Low	1	0	1	1	0	1	0	X
	A6	A5	A4	A3	A2	A1	A0	R/W																					
High	1	0	1	1	0	1	1	X																					
Low	1	0	1	1	0	1	0	X																					
6	MUTE	The mute input, when asserted, will mute the SDAT output samples. It sets the sample values to zero. In non-I ² C applications, this input is active low. With the I ² C active, the mute polarity can be set to an "exclusive-or" operation with the SC3 bit. See fig 2.																											
7	TEST	This pin must be connected to VSS for normal operation.																											
8	STIM	Sound bus output timing signal. Depending on the bus format selected, either I ² S's word select (I ² SWS) or S-bus's sound identification (S-ident). This output can be set to tri-state via I ² S.																											
9	SCLK	Sound bus output clock. Depending on the bus format selected either I ² S's I ² SCK or S-Bus's S-clock @ 5.824 Mbits/s. This output can be set to tri-state via I ² C.																											
10	SDAT	Sound bus data output pin. Depending on the bus format selected (via BFSEL) this pin carries either I ² S's I ² SD or S-bus's S-DATA serial data output. This output can be set tri-state via I ² C.																											
11,25	SDAT CONTD	Ground (0v).																											
12	VSS BFSEL	Input for the selection of the sound output bus format. <div style="display: flex; justify-content: space-around;"><div>BFSEL</div><div>BUS Format</div></div> <table style="margin-left: auto; margin-right: auto;"><tr><td>High</td><td>S-bus</td></tr><tr><td>Low</td><td>I²S bus</td></tr></table> When S-bus is selected the oversampling function is automatically turned off.	High	S-bus	Low	I ² S bus																							
High	S-bus																												
Low	I ² S bus																												
13	DMSEL	An active high "dual mono select" input. When asserted, this input will select M1 and M2 as the output signals when the incoming transmission consists of two independent mono signals.																											
14	M1/M2	An "M1 or M2" select input. This input will select either M1 (M1/M2=1) or M2 (M1/M2=0) when the input transmission consists of two independent mono signals. See fig 2.																											
15	RESET	Active low reset input. Used to set the device in a valid initial condition e.g. at power on.																											
16	XOUT	Respectively the output and input of a single stage inverter																											
17	XIN	Used to provide a crystal oscillator maintaining circuit (with external biasing) or a simple CMOS input at XIN for the 17.472 MHz master clock.																											
19	PCLK	Output 728 KHz clock derived from the 17.472 MHz crystal																											
20	EDET	Active high error detect output. It indicates that an output sample is unreliable (having been obtained by interpolation).																											
21	DATA	Serial data at 728 kbits/s from the DQPSK demodulator.																											
22	LAST	Logical "AND" status pin, which gives the status of VDSP. (RSSF+FLO). See fig 2. VDSP, "valid digital sound present" signal. When high, this output indicates that the decoder is operating with a valid NICAM digital input which carries at least one sound channel.																											
	LAST contd	RSSF "or" FLO FLO is a RSSF over-ride signal which allows a user to turn off the RSSF input to the 'LAST' function. The purpose of this is to disable the RSSF input to the logical AND																											