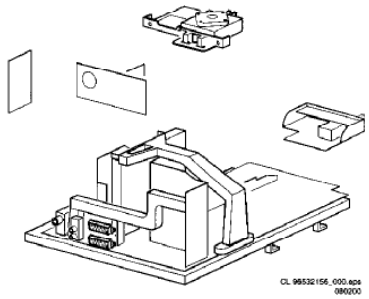
Colour television

Chassis

EM2E

AA

Service
Service
Service



Service Manual

Published by CO 0061 Service PaCE | Printed in the Netherlands | Subject to modification | GB 3122 785 10310

PHILIPS

protection will take place if the SDA and SCL are whether short circuited to ground or to each other. An I^2C error can also occur, if the power supply of the IC is missing (e.g. TUNER_PROT (error 12) & FBX_PROT (error 16)).

OTC related protections

If a protection is detected at an input of the OTC, all protection inputs of the OTC will be scanned every 200 msec. for 5 times. If the protection on one of the inputs is still activated after 1 sec., then the set will be put in the protection-mode. Before the scanning is started a so-called ESD-refresh will be carried out first, because the interrupt on one of the inputs may be caused either by a FLASH or by ESD. As a FLASH or ESD can harm the settings of some IC's, the HOP-HIP-MSP-PICNIC-NVM and Tuner are initialised again to ensure the normal picture and sound conditions of the set.

- 8.6 V and 5.2 V protection. The presence of the 8.6 V and 5.2 V is sensed by the OTC. If these voltages are not present, then an error code is stored in the error buffer of the NVM, and the set is put in the protection-mode.

HOP related protections

Every 200 msec. the status register of the HOP is read by the OTC via I^2C. If a protection signal is detected on one of the inputs of the HOP, then the relevant error bit in the HOP register is set to 'high'. If the error bit is still 'high' after 1 sec., the OTC will store the error code in the error buffer (NVM) and depending on the relevancy of the error bit the set will either go into the protection-mode or not.

- HFB: Horizontal Flyback. If the horizontal flyback is not present, then this is detected via the HOP (HFB_X-RAY_PROT). One status bit is set to 'high'. The error code is stored in the error buffer and the set will go into the protection mode
- Flash detection. From the EHT-info, via D6303 and T7303 a flash will stop the H-drive and line output stage immediately. The FLS-bit in the status register of the HOP is set to 'high'. As the duration of a flash is very short the FLS-bit will be reset to 'low' again after the flash refresh, so via a slow start the set will be started again.

Hardware related protections

Due to the architecture (with 'hot' deflection) there are two protections that are 'unknown' to the microprocessor, namely the 'BRIDGE_PROT' from the line-stage and the 'NO_VFB' protection form the frame-stage. If one of these protections is triggered, the set is positioned in 'Standby'-mode. The OTC will now try to re-start the set. If this will not succeed after 5 times (after ≈ 1 minute), the OTC will generate error 15 (Flash protection) and will start the blinking red LED.

5.7.2 Repair tips

Phenomenon	Possible Cause	Repair-tip
No picture, no LED.	Standby Supply defective.	Measure circuitry (see diagram A2). Start at testpoint P16. Regardless the mode of the set, this voltage should always be available.
No picture, red LED (high intensity) despite expectation the set should be 'on' (this looks like Standby).	There are 2 protections that are not 'seen' by processor, that force set in 'Standby'-mode, namely 'NO-VFB-prot' (= no frame-deflection), or 'BRIDGE_PROT' (safety error).	If protection is activated by 'NO_VFB-prot', this can be measured with a scope on service test point F10 (diagram A4). Before this protection is activated, a few seconds a horizontal white line is visible. The 'BRIDGE_PROT' error may never occur. Is implemented due to legal requirements. Flash protection error (15) will be generated in both cases after 5 restart attempts. Visible via blinking LED procedure. NO_VFB-prot can be determinated by white line.
No picture, red LED blinking (3 Hz).	Set is in protection due to various causes. For error codes see error-code list.	You have no picture, so: - or you read out error buffer via ComPair - or you read out blinking LED information via 'diagnose' x dealer remote - or you read out blinking LED sequence via <default>-button dealer remote - or you read out blinking LED sequence via service default mode entered via RC-command 062596 + 'menu' When error is known, check circuitry related to supply-voltage and I^2C-communication.
No picture, red LED blinking code 6,6,6 or 1,1,1	No communication on I^2C-bus or NVM-I^2C-bus to processor. Set is in protection-mode	As processor cannot communicate with one of the 2 busses it spontaneously starts blinking. Measure dependent of the error on the I^2C-bus which device is loading the bus. This protection can be overruled via SDM-entry on SSB or via stepwise start-up mode step 'MainPowerOn'.
No picture, no sound, set is making audible squeaking sound	Supply could be in hiccup-mode which can be heard via supply-transformer squeaking	This could be caused by: - Short-circuited V_{BAT} (caused by short circuited line transistor 7421) or - Short-circuited sound-winding (amplifier is short-circuiting 28 V) or - Short-circuited D6514 (due to a too high V_{BAT}). Delete excessive load to see where failure is caused by or check feed back circuit. See repair-tip main power supply (supply needs a minimal load).
No picture, no sound, LED works fine	Supply does not work correctly	If e.g. V_{BAT} is only about 90 V, regulator-IC 7506 could be damaged.
No RC5-reception. Red LED does not echo RC-commands.	Processor-circuitry or RC-receiver is wrong.	In case set reacts on local keyboard operation, error must be found in the IR-receiver circuitry (diagram E).
Relay-activation (degaussing) not audible when switch set 'on' from 'off'.	Processor not working correctly.	Check RESET-circuitry on diagram B5. When switching on the set all i/o-pins of processor should become high for a moment, so also the degauss-input signal.
No sound, but picture.	Measure P7 on diagram A1. Possible sound-amplifier is broken (but not short-circuited), or sound-enable line is high (see diagram A5). Further the audio-signal path must be measured (HIP, MSP, switch-IC's, amplifier).	Measure and repair. With ComPair there is a beep-test that can determine where the signal stops (use loudspeakers, headphone).
No sound at headphone output.	Discrete amplifiers or supply to it could be damaged.	Measure A12, A13, A14, A15 and supply-line on diagram A6.
Picture is rotated.	Rotation-circuitry or supply to it could be damaged.	Measure test points F3, R1, R2 on diagram A4.
No picture.	Check functionality and cabling Tuner to SSB.	Notice cable 0946.
Picture looks like cushion, further O.K.	Or NVM-content is overwritten or E/W-MOSFET is short-circuited	First check in Service Alignment Mode, whether geometry can be restored. If not check testpoint L4 and diagram A3, or measure with an ohm-meter whether TS7480 is defective.
Very white picture, with flyback lines visible	180 V is missing on CRT-panel	Probably R3468 on LSP (diagram A3) is interrupted, or bad connection plug 0324 to 0224 (CRT-panel).
Un-sharp picture	Focus could be mis-aligned or SCAVEM-circuitry does not work correctly	Align focus-potmeter of Line Transformer; check SCAVEM-circuitry on CRT-panel [F].
Un-synced picture	Sync is derived in HIP-IC from X-tals 1305 and/or 1308	Maybe a X-tal is making bad contact.
Picture distorted.	Check video-path, service default mode.	Investigate whether there exist an error code in the error buffer. In case there is an error code, check I^2C-bus and/or supply-lines (see overview supply-lines). Measure and check signal path Tuner, HIP, PICNIC, HOP, RGB-amplifier. In case it is a geometry-issue, check Frame-circuitry, alignments or possible corrupted NVM (7011)
No menu, OSD.	Probably processor is defective.	Measure test points C7, C8, C9, C10 on diagram B5.

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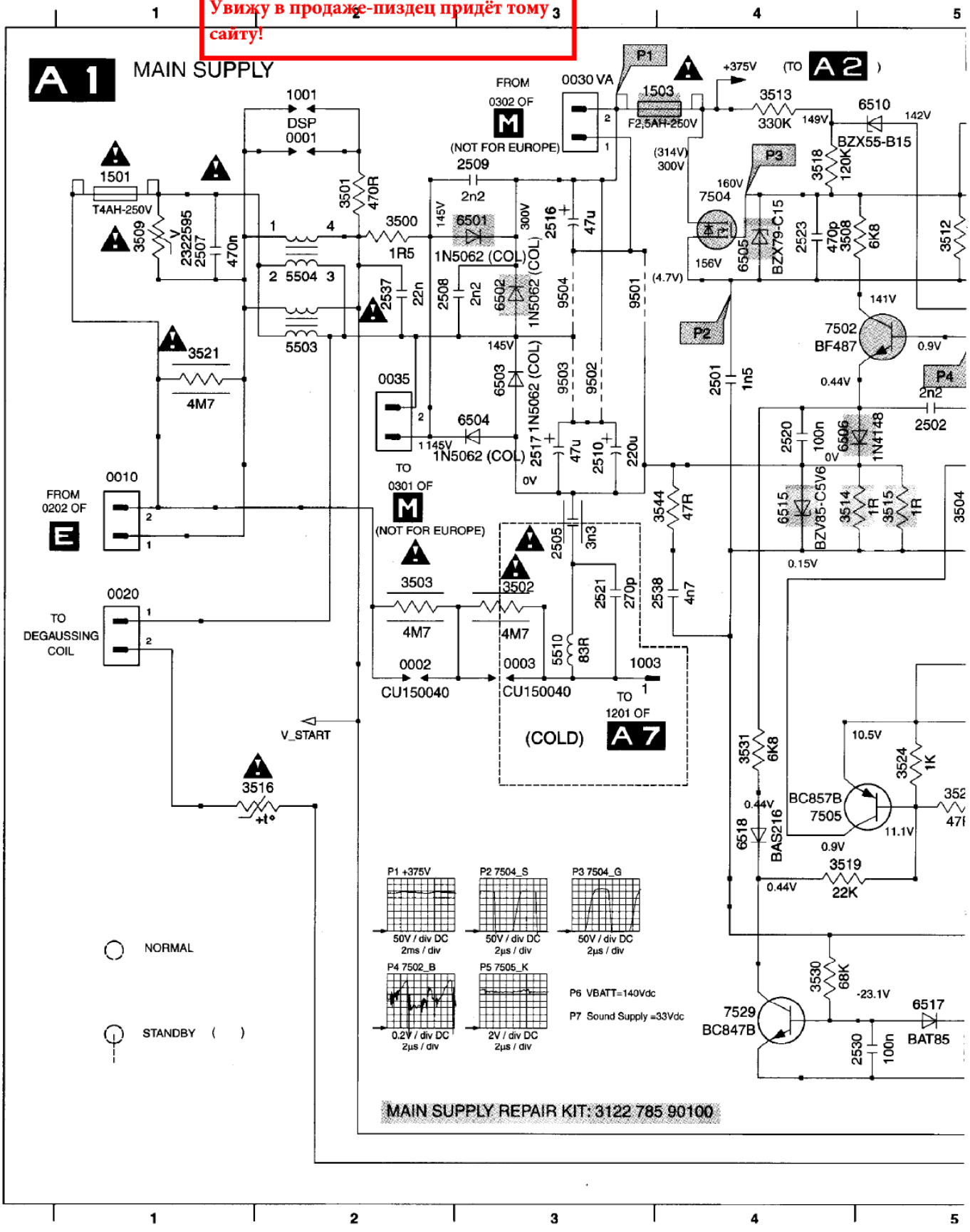
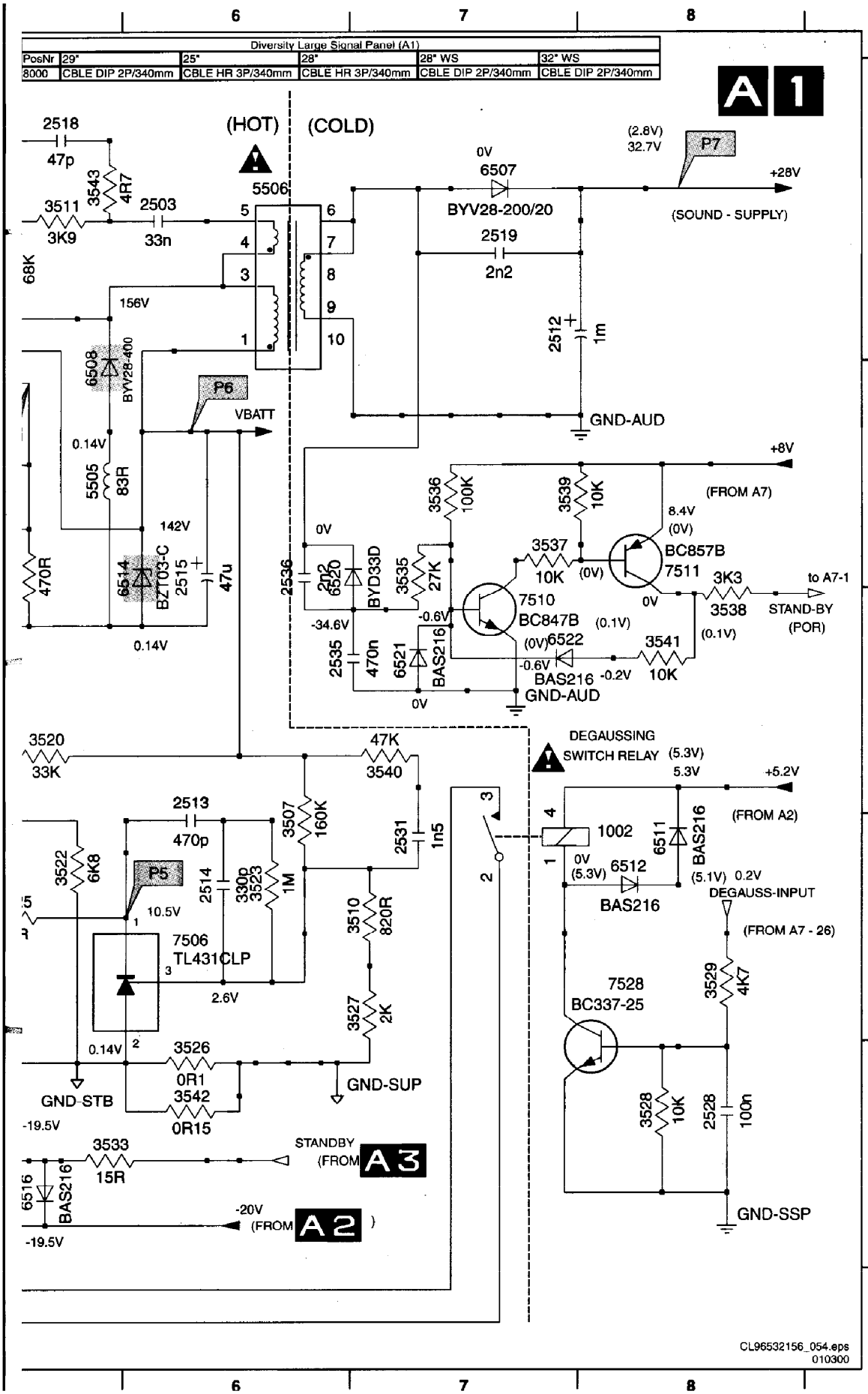
7. Schematics and PWB's

Main supply

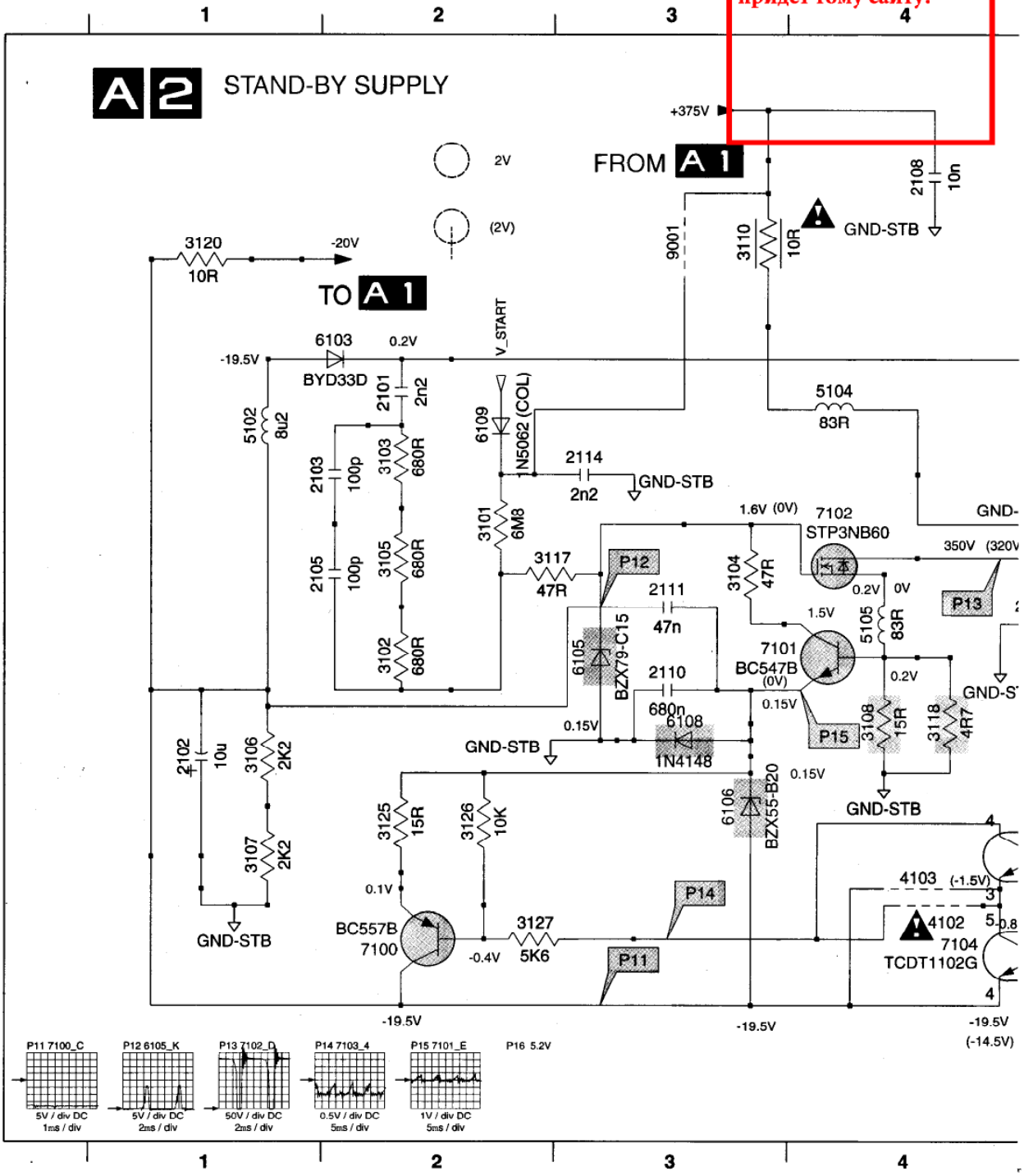


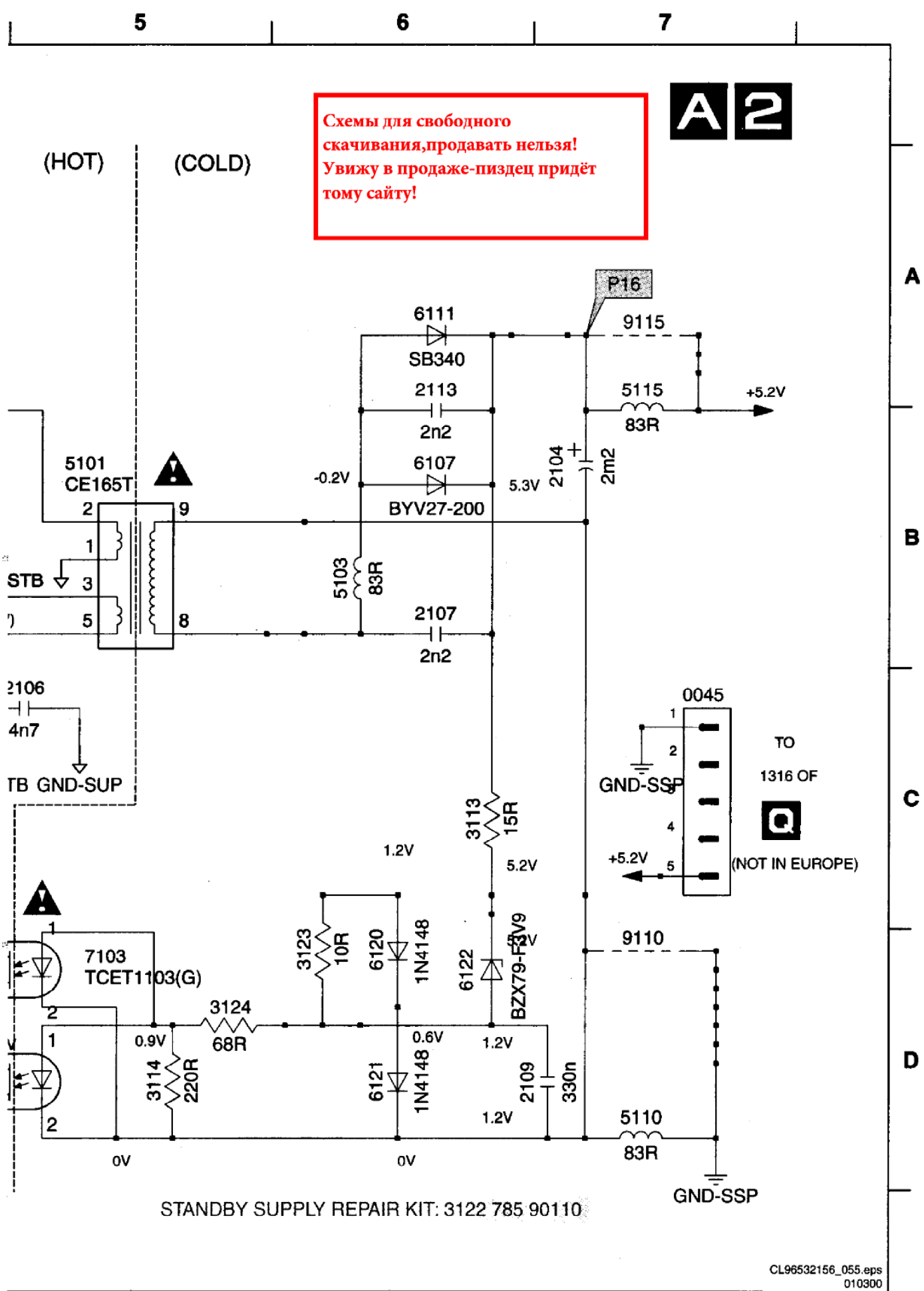


	0001 A2	3537 B7
	0002 C2	3538 C8
	0003 C3	3539 B7
	0010 B1	3540 C7
	0020 C1	3541 C8
	0030 A3	3542 E6
	0035 B2	3543 A5
	1001 A2	3544 B4
	1002 D8	5503 B2
	1003 C4	5504 A2
A	1501 A1	5505 B5
	1503 A4	5506 A6
	2501 B4	5510 C3
	2502 B5	6501 A3
	2503 A6	6502 A3
	2505 C3	6503 B3
	2507 A1	6504 B3
	2508 A2	6505 A4
	2509 A3	6506 B4
	2510 B3	6507 A7
	2512 A7	6508 B5
	2513 C6	6510 A5
	2514 D6	6511 D8
B	2515 B6	6512 D8
	2516 A3	6514 B6
	2517 B3	6515 B4
	2518 A5	6516 E5
	2519 A7	6517 E5
	2520 B4	6518 D4
	2521 C3	6520 B6
	2523 A4	6521 C7
	2528 E8	6522 C7
	2530 E5	7502 B5
	2531 D7	7504 A4
	2535 C6	7505 D4
C	2536 B6	7506 D6
	2537 A2	7510 C7
	2538 C4	7511 B8
	3500 A2	7528 D8
	3501 A2	7529 E4
	3502 C3	9501 A3
	3503 C2	9502 B3
	3504 B5	9503 B3
	3507 D6	9504 A3
	3508 A4	
	3509 A1	
	3510 D7	
D	3511 A5	
	3512 A5	
	3513 A4	
	3514 B4	
	3515 B5	
	3516 D2	
	3518 A4	
	3519 D4	
	3520 C5	
	3521 B1	
	3522 D5	
E	3523 D6	
	3524 D5	
	3525 D5	
	3526 E6	
	3527 D7	
	3528 E8	
	3529 D8	
	3530 E4	
	3531 D4	
	3533 E5	
	3535 B7	
	3536 B7	

Standby supply

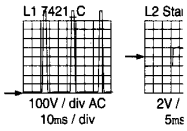
0045 C7	2107 B6	3101 B2	3108 C4	3123 D6	5101 B5	6103 A2	6120 D6
2101 B2	2108 A4	3102 C2	3110 A3	3124 D5	5102 B1	6105 C3	6121 D6
2102 C1	2109 D7	3103 B2	3113 C6	3125 D2	5103 B6	6106 C3	6122 D6
2103 B2	2110 C3	3104 B3	3114 D5	3126 D2	5104 B4	6107 B6	7100 D2
2104 B7	2111 C3	3105 B2	3117 B2	3127 D2	5105 C4	6108 C3	7101 C4
2105 B2	2113 A6	3106 C1	3118 C4	4102 D4	5110 D7	6109 B2	7102 B4
2106 C5	2114 B3	3107 D1	3120 A1	4103 D4	5115 A7	6111 A6	7103 D5

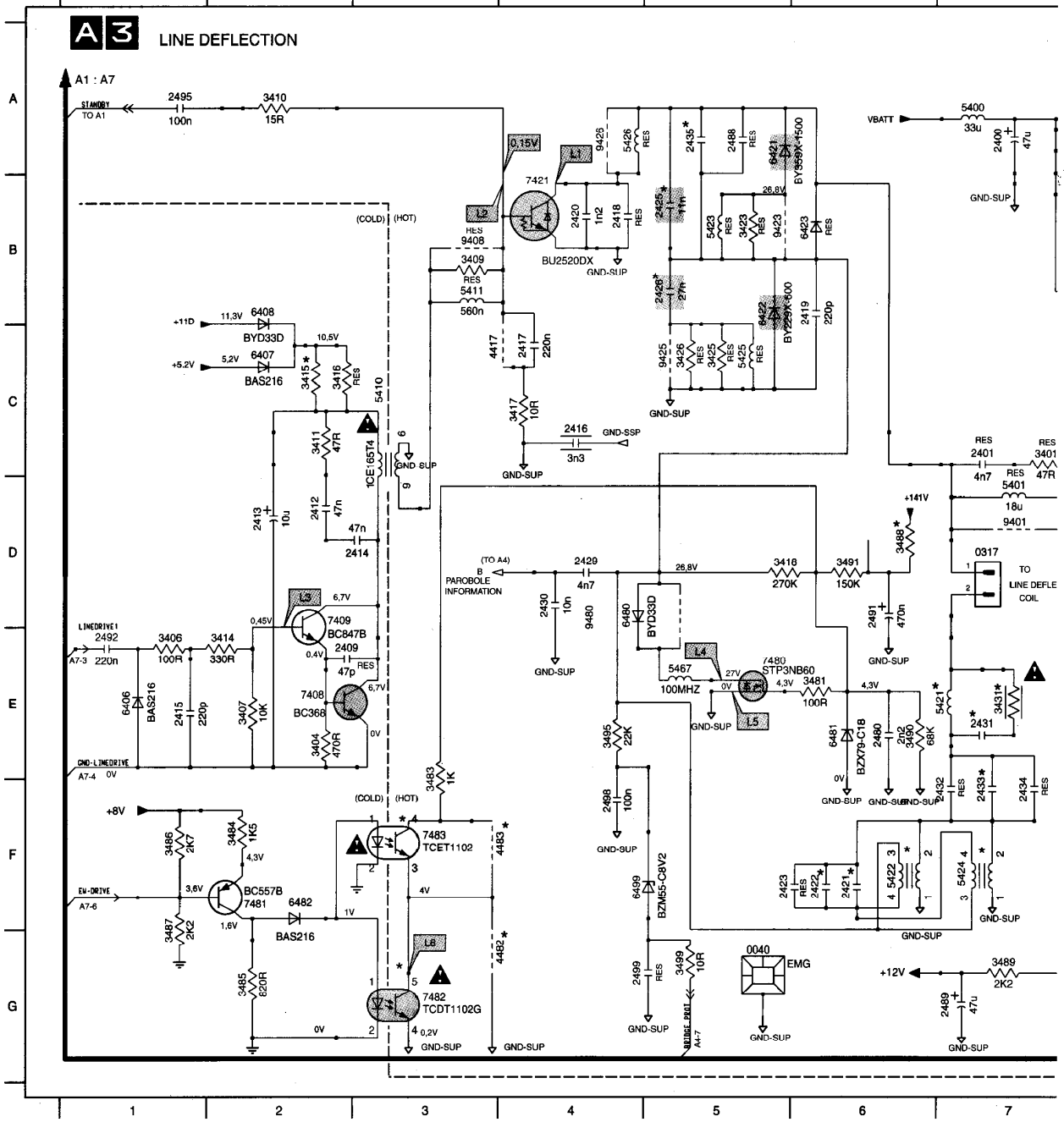


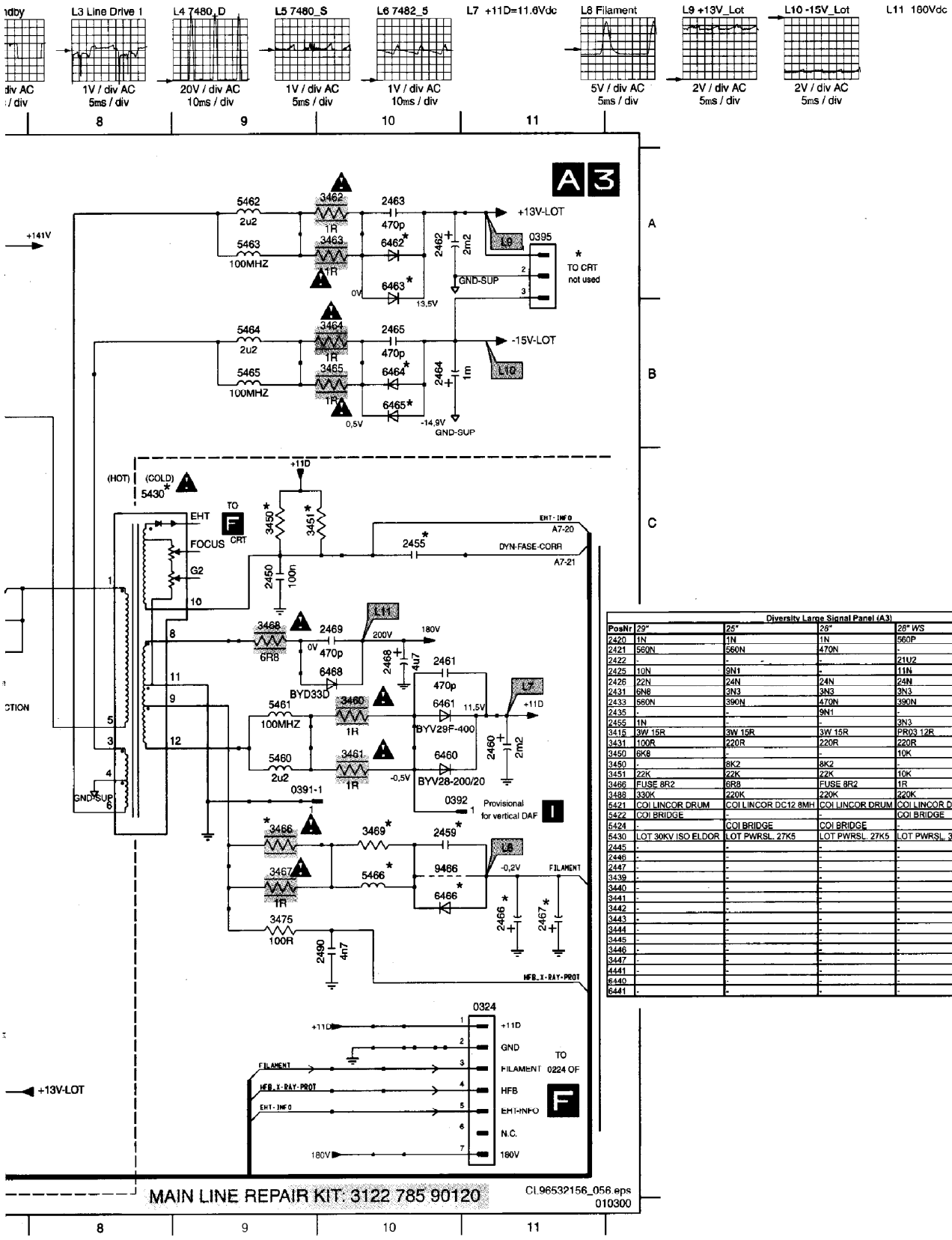


Line deflection

2400 A7	2421 F6	2450 C9	2469 D10	3406 E1	3426 C5	3468 D9	3491 D6	5423 B5	5467 E5	6465 B10	7482 G3
2401 C7	2422 F6	2455 C10	2480 E6	3407 E2	3431 E7	3469 E10	3495 E4	5424 F7	6406 E1	6466 F10	7483 F3
2409 E2	2423 F5	2459 E10	2488 A5	3409 B3	3450 C9	3475 F9	3499 G5	5425 C5	6407 C2	6468 D10	9401 D7
2412 D2	2425 B5	2460 D11	2489 G7	3410 A2	3451 C9	3481 E6	4417 C3	5426 A4	6408 B2	6480 D4	9408 B3
2413 D2	2426 B5	2461 D10	2490 F10	3411 C2	3460 D10	3483 F3	4482 G3	5430 C8	6421 A5	6481 E6	9423 B5
2414 D3	2429 D4	2462 A10	2491 D6	3414 E2	3461 E10	3484 F2	4483 F3	5460 E9	6422 B5	6482 F2	9425 C5

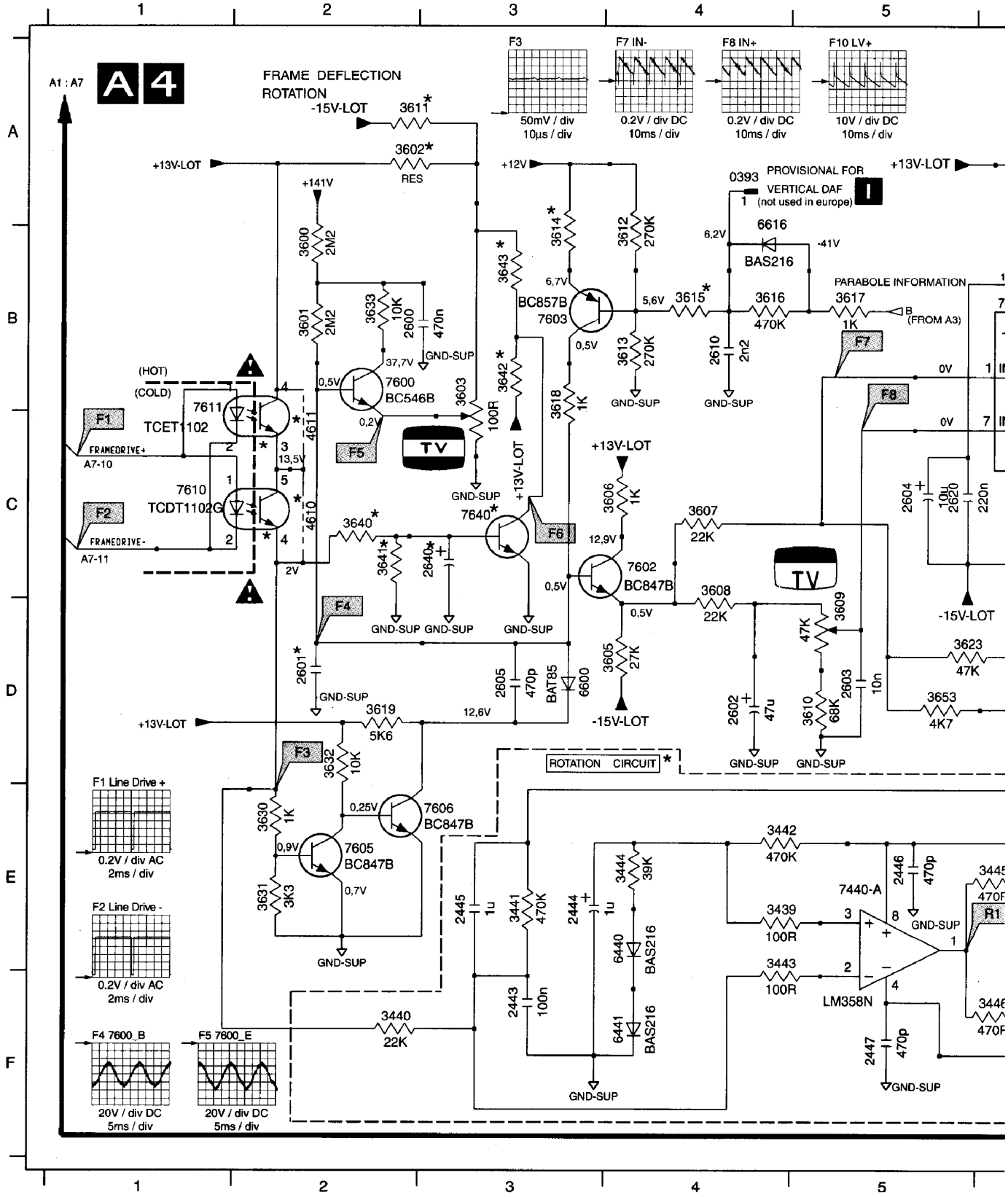


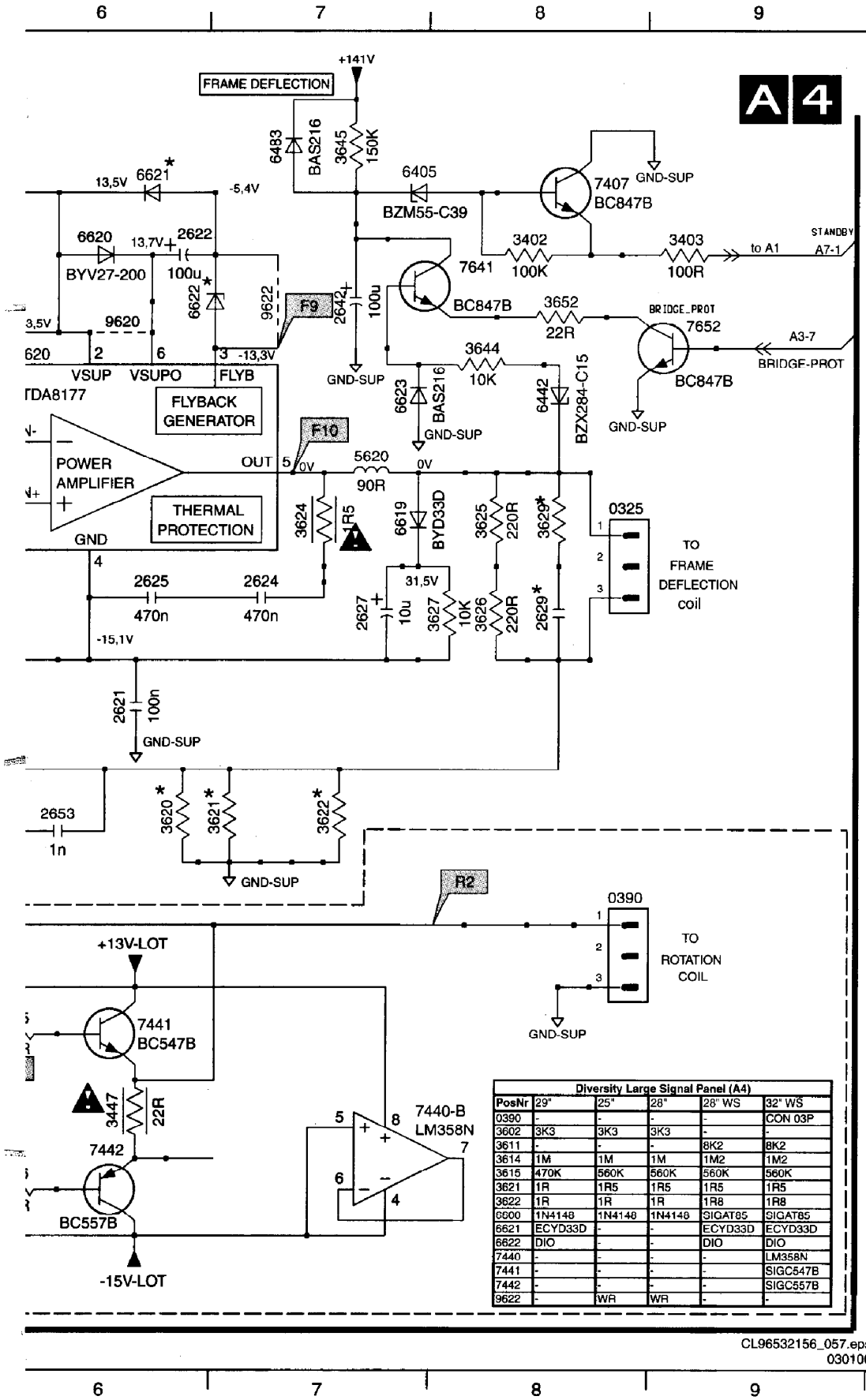




Diversity Large Signal Panel (A3)					
PosNr	29"	25"	26"	26" WS	32" WS
2420	1N	1N	1N	560P	1N
2421	560N	560N	470N	-	-
2422	-	-	-	21U2	21U2
2425	10N	9N1	-	11N	11N
2426	22N	24N	24N	24N	24N
2431	6N8	3N3	3N3	3N3	3N3
2433	560N	390N	470N	390N	430N
2435	-	-	9N1	-	-
2455	1N	-	-	3N3	3N3
3415	3W 15R	3W 15R	3W 15R	PR03 12R	PR03 12R
3431	100R	220R	220R	220R	220R
3450	6K8	-	-	10K	10K
3450	-	8K2	8K2	-	-
3451	22K	22K	22K	10K	10K
3466	FUSE 8R2	6R8	FUSE 8R2	1R	1R
3498	330K	220K	220K	220K	120K
5421	COI LINCOR DRUM	COI LINCOR DC12 8MH	COI LINCOR DRUM	COI LINCOR DRUM	COI LINCOR DRUM
5422	COI BRIDGE	-	-	COI BRIDGE	COI BRIDGE
5424	-	COI BRIDGE	COI BRIDGE	-	-
5430	LOT 30KV ISO ELDOR	LOT PWRSL. 27K5	LOT PWRSL. 27K5	LOT PWRSL. 30KV	LOT PWRSL. 30KV
2445	-	-	-	-	1U
2446	-	-	-	-	470P
2447	-	-	-	-	470P
3439	-	-	-	-	100R
3440	-	-	-	-	22K
3441	-	-	-	-	470K
3442	-	-	-	-	470K
3443	-	-	-	-	100R
3444	-	-	-	-	39K
3445	-	-	-	-	2K2
3446	-	-	-	-	2K2
3447	-	-	-	-	22R
4441	-	-	-	-	JUMP
6440	-	-	-	-	SMAS216
6441	-	-	-	-	SMAS216

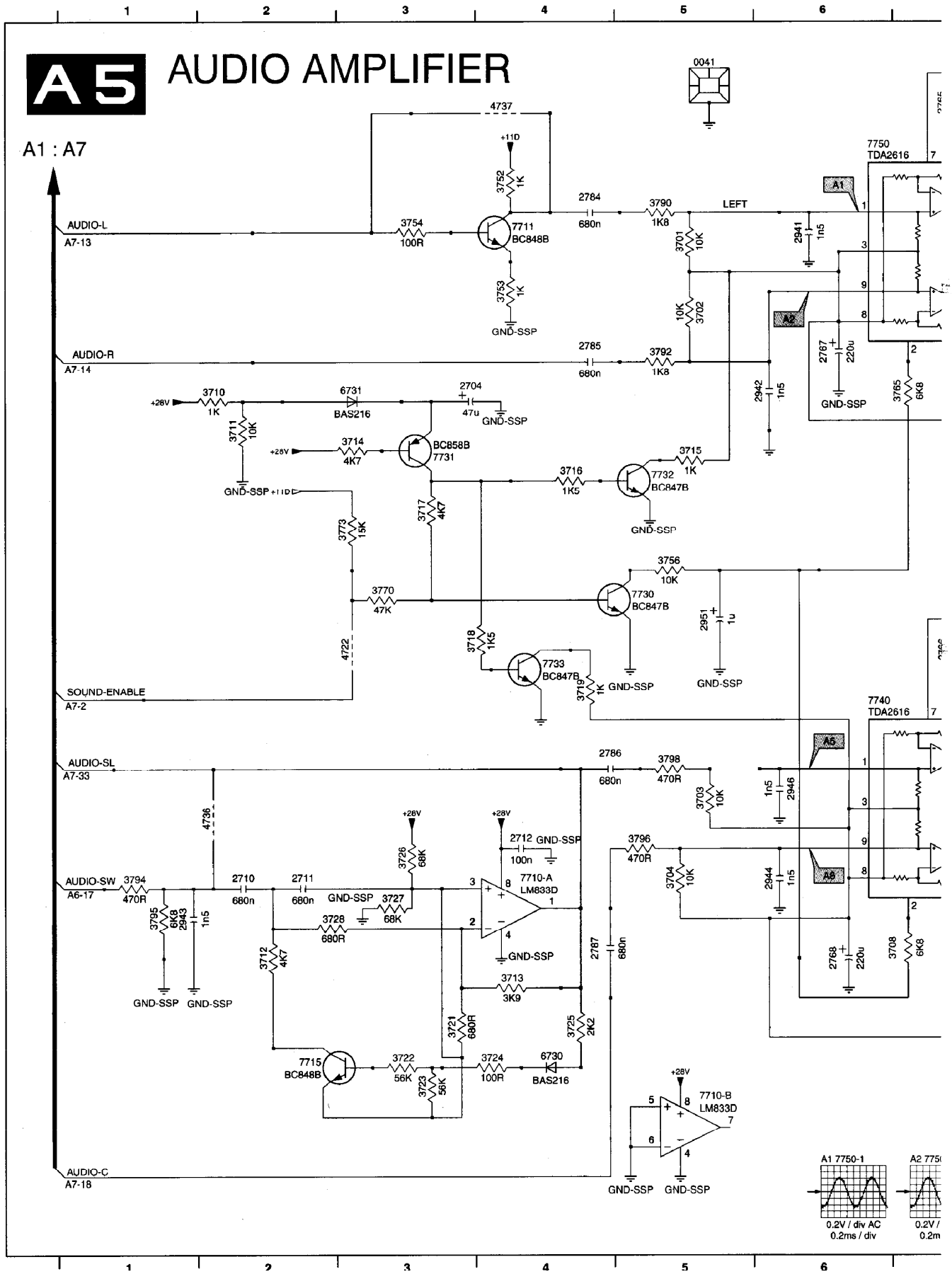
Frame deflection

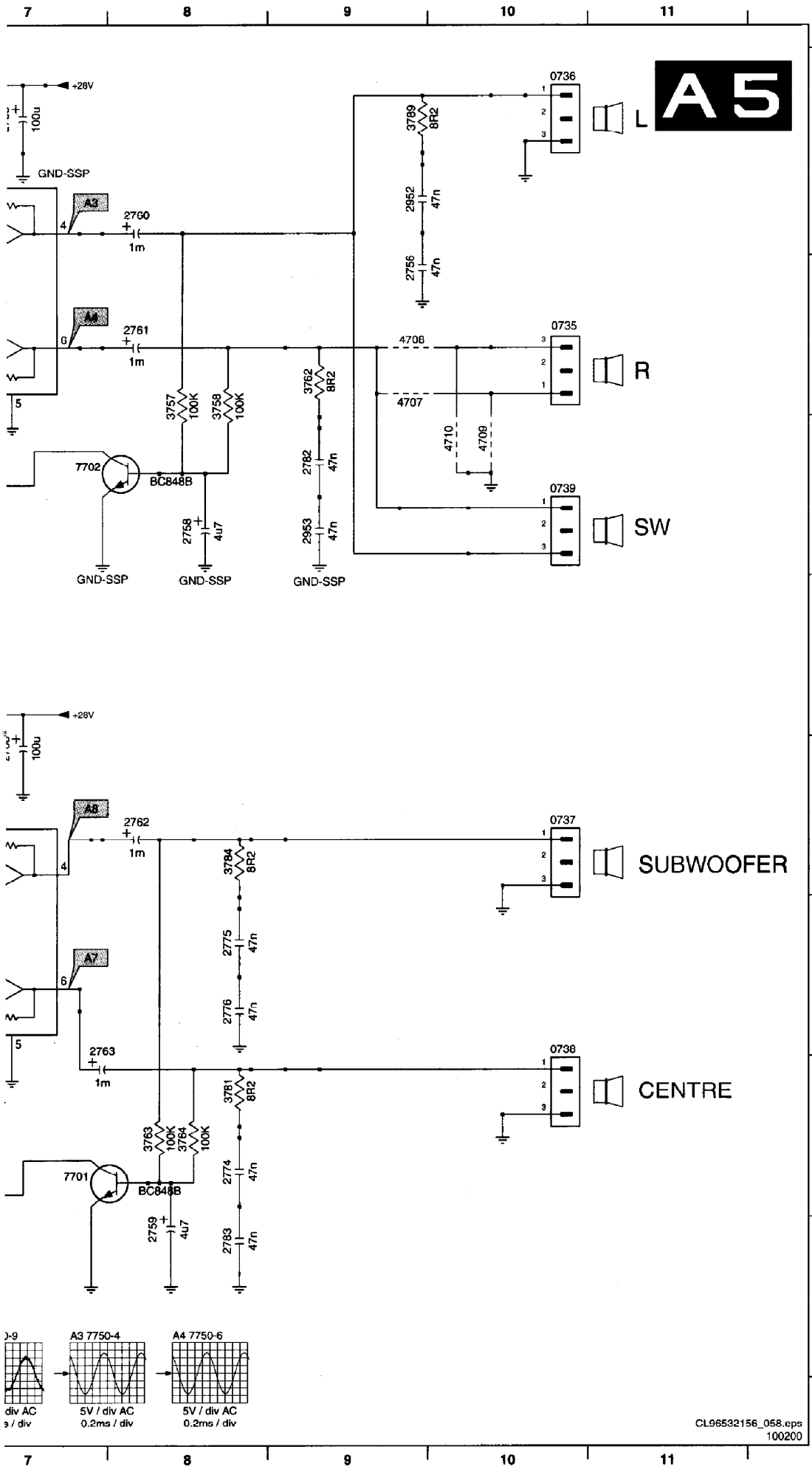




PosNr	29"	25"	28"	28" WS	32" WS
0390	-	-	-	-	CON 03P
3602	3K3	3K3	3K3	-	-
3611	-	-	-	8K2	8K2
3614	1M	1M	1M	1M2	1M2
3615	470K	560K	560K	560K	560K
3621	1R	1R5	1R5	1R5	1R5
3622	1R	1R	1R	1R8	1R8
6600	1N4148	1N4148	1N4148	SIGAT85	SIGAT85
6621	ECYD33D	-	-	ECYD33D	ECYD33D
6622	DIO	-	-	DIO	DIO
7440	-	-	-	-	LM358N
7441	-	-	-	-	SIGC547B
7442	-	-	-	-	SIGC557B
9622	-	WR	WR	-	-

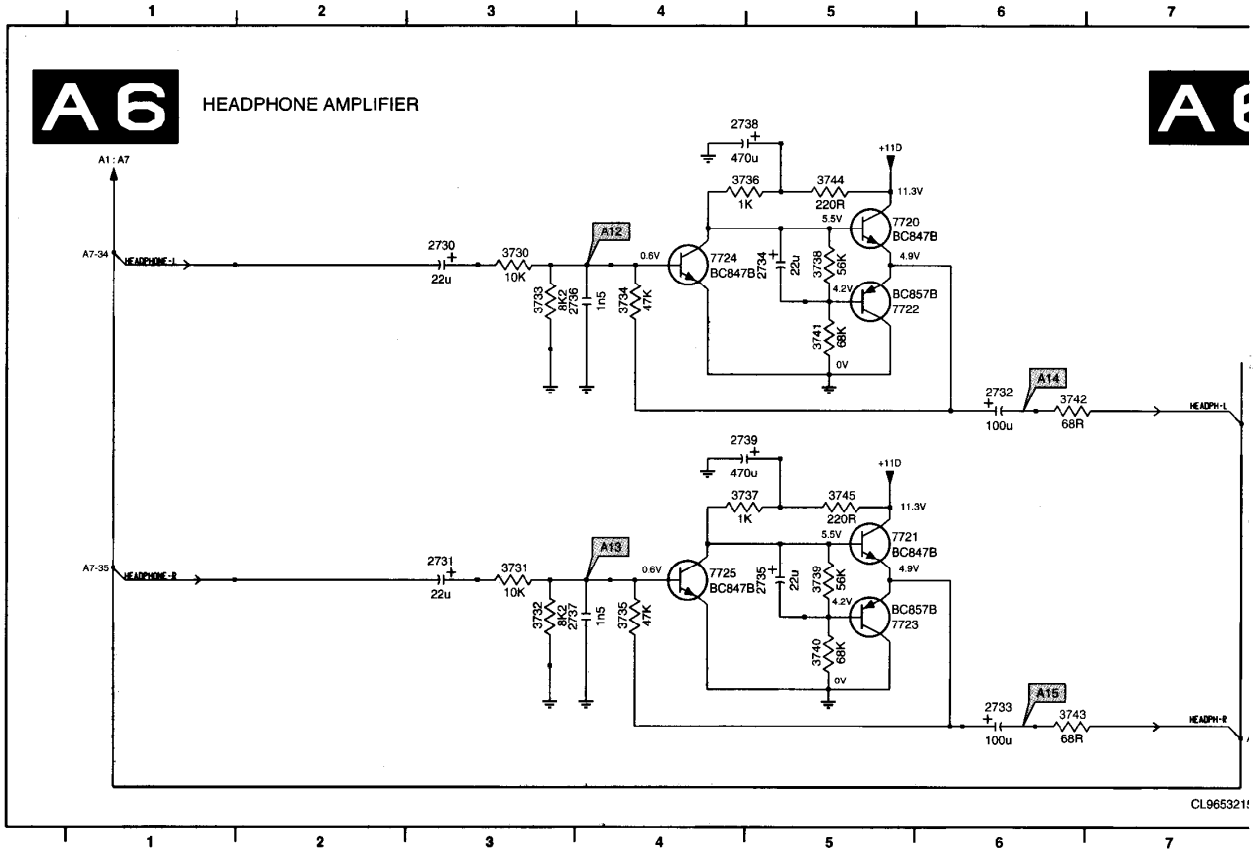
Audio amplifier



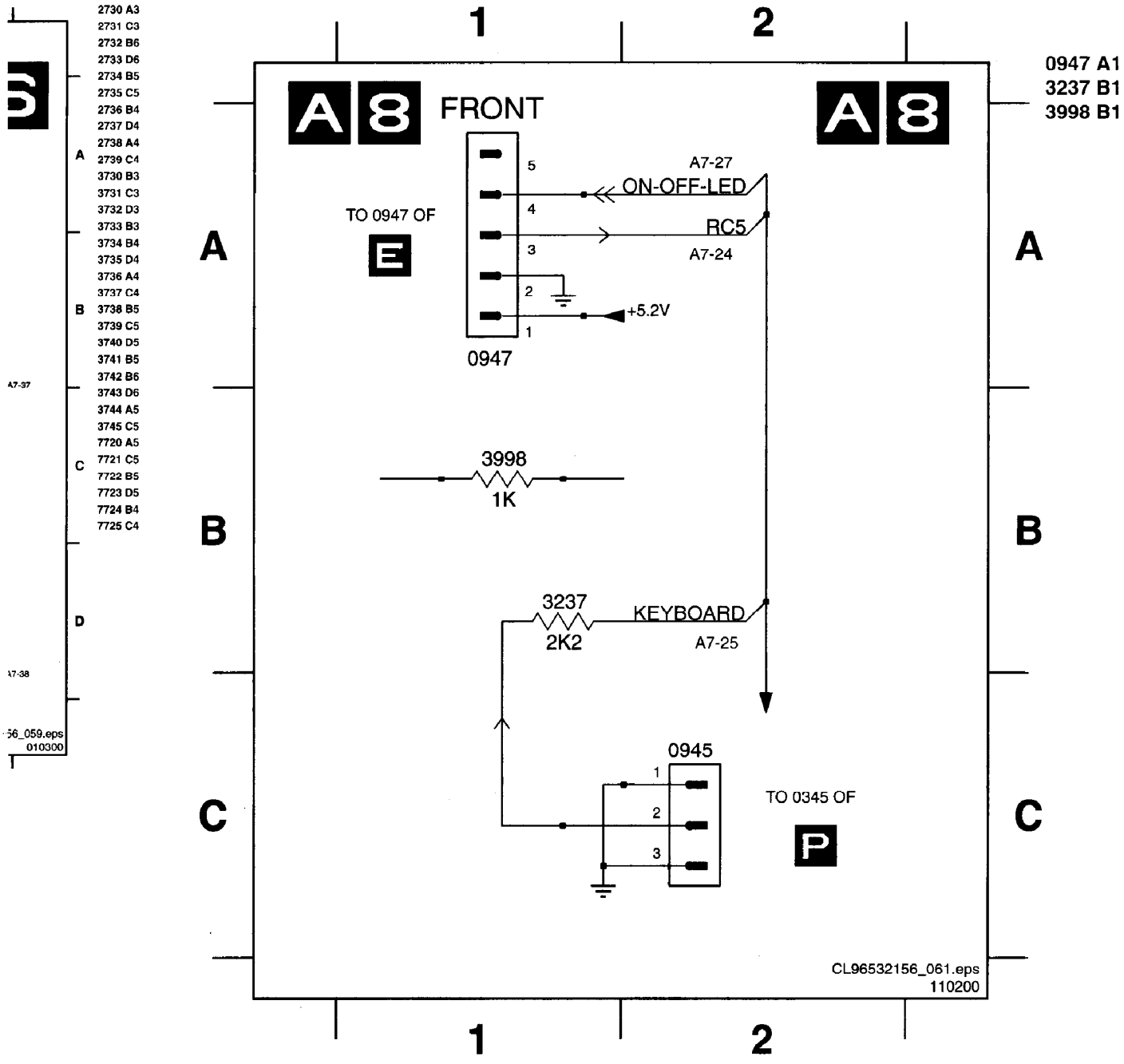


0041 A5
0735 B10
0736 A10
0737 E10
0738 F10
0739 C10
2704 C3
2710 F2
2711 F2
2712 F4
2756 B9
2758 C8
2759 H8
2760 A8
2761 B8
2762 E8
2763 F7
2765 A7
2766 E7
2767 B6
2768 G6
2774 G8
2775 F8
2776 F8
2782 C9
2783 H8
2784 A4
2785 B4
2786 E4
2787 G4
2941 B6
2942 C6
2943 G1
2944 F6
2946 F6
2951 D5
2952 A9
2953 C9
3701 B5
3702 B5
3703 F5
3704 F5
3708 G7
3710 C2
3711 C2
3712 G2
3713 G4
3714 C3
3715 C5
3716 C4
3717 D3
3718 E3
3719 E4
3721 G3
3722 H3
3723 H3
3724 H4
3725 G4
3726 F3
3727 F3
3728 G2
3752 A4
3753 B4
3754 B3
3756 D5
3757 B8
3758 B8
3762 B9
3763 G8
3764 G8
3765 C7
3770 D3
3773 D3
3781 G8
3784 E8
3789 A9
3790 A5
3792 B5
3794 F1
3795 G1
3796 F5
3798 E5
4707 B9
4708 B9
4709 C10
4710 C10
4722 E3
4736 F2
4737 A4
6730 H4
6731 C3
7701 G7
7702 C7
7710-A F4
7710-B H5
7711 B4
7715 H2
7730 D5
7731 C3
7732 C5
7733 E4
7740 E6
7750 A6

Headphone amplifier



Front


2730 A3
2731 C3
2732 B6
2733 D6
2734 B5
2735 C5
2736 B4
2737 D4
2738 A4
2739 C4
3730 B3
3731 C3
3732 D3
3733 B3
3734 B4
3735 D4
3736 A4
3737 C4
3738 B5
3739 C5
3740 D5
3741 B5
3742 B6
3743 D6
3744 A5
3745 C5
7720 A5
7721 C5
7722 B5
7723 D5
7724 B4
7725 C4
A7-37
A7-38
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010300
1
2
A
B
C
A8
FRONT
A8
0947 A1
3237 B1
3998 B1
TO 0947 OF
E
5
4
3
2
1
A7-27
ON-OFF-LED
RC5
A7-24
+5.2V
0947
3998
1K
3237
2K2
KEYBOARD
A7-25
0945
TO 0345 OF
P
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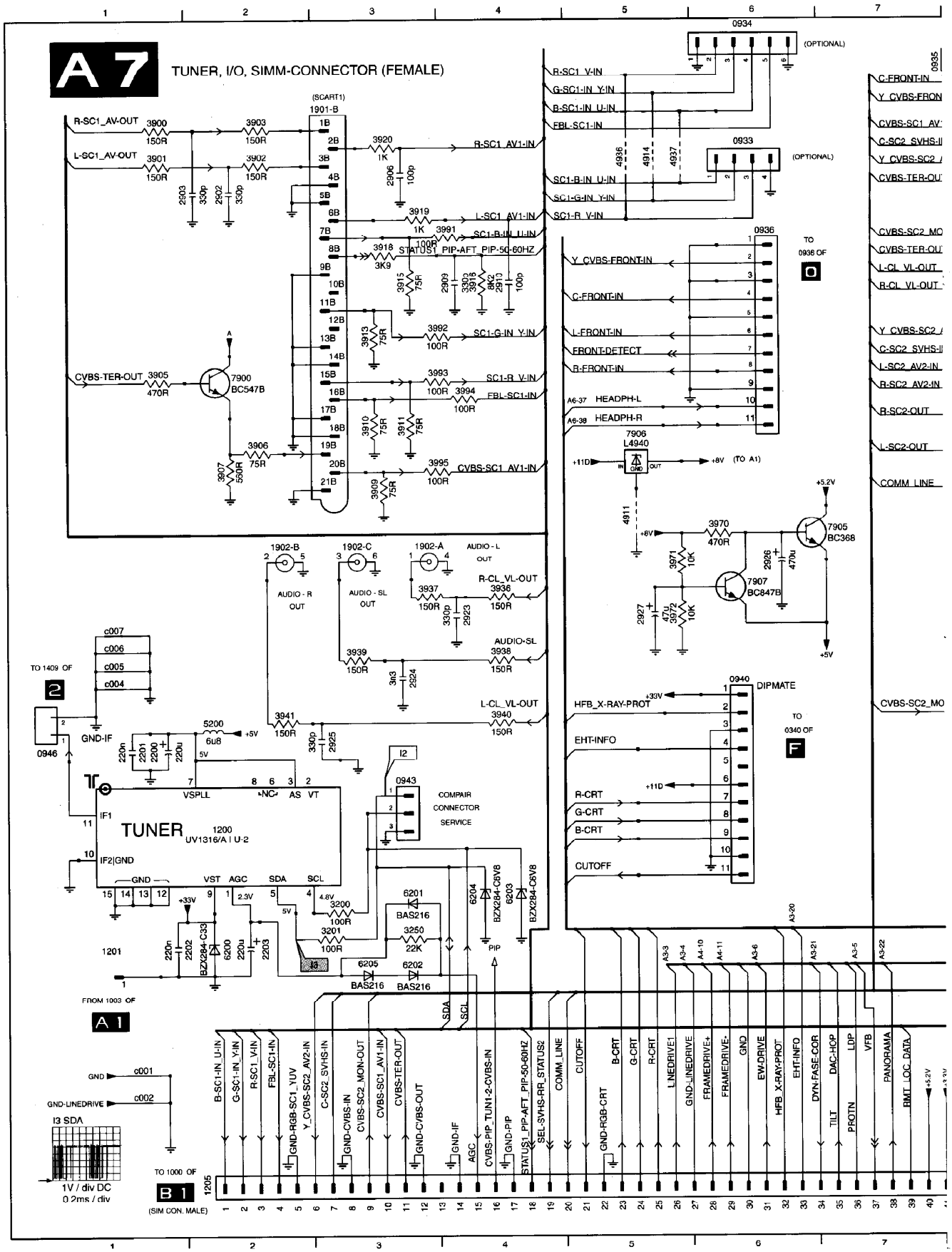
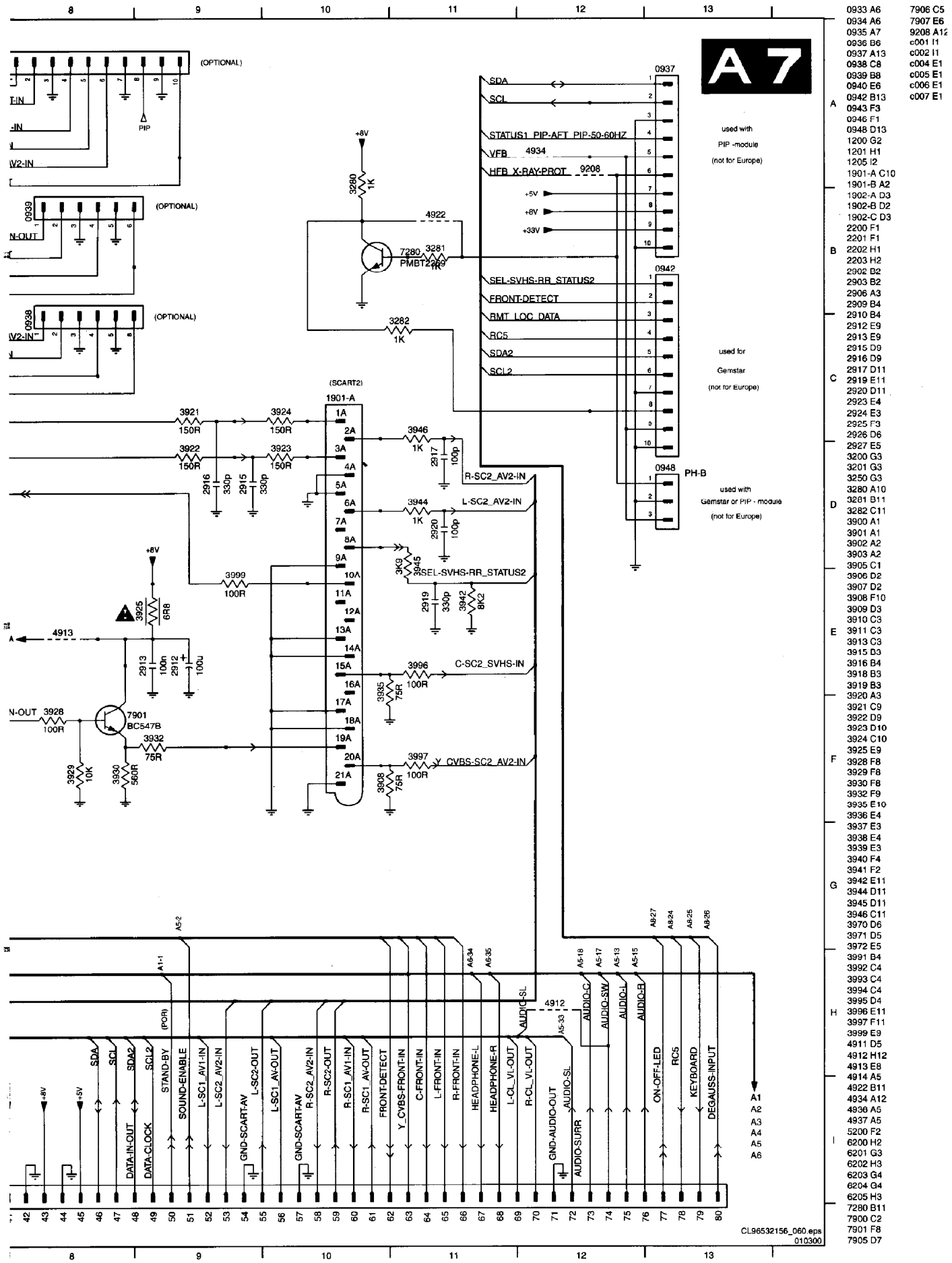
110200

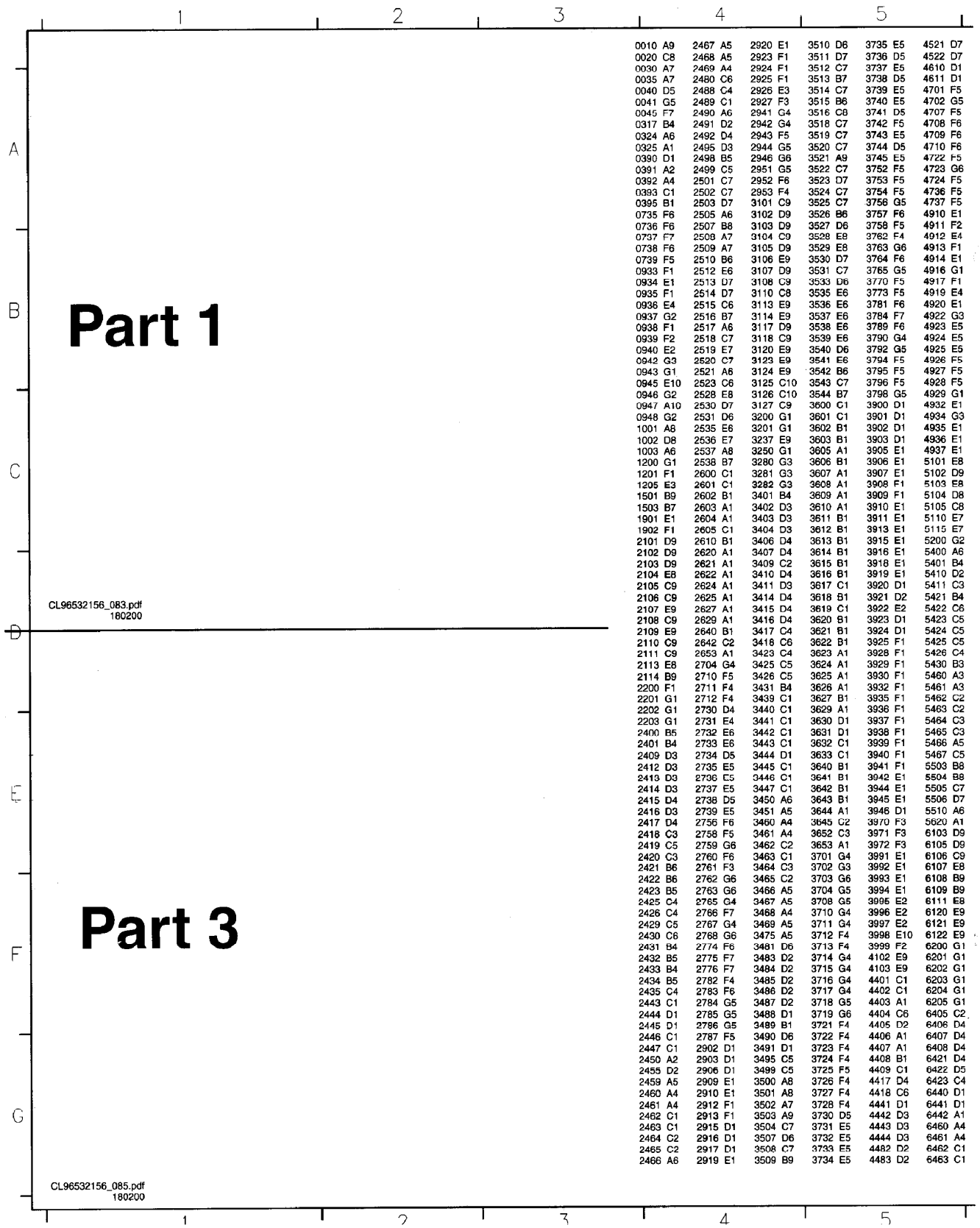
Tuner, I/O, Simm connector (female)





0933 A6 7906 C5
0934 A6 7907 E6
0935 A7 9208 A12
0936 B6 c001 I1
0937 A13 c002 I1
0938 C8 c004 E1
0939 B8 c005 E1
0940 E6 c006 E1
0942 B13 c007 E1
0943 F3
0946 F1
0948 D13
1200 G2
1201 H1
1205 I2
1901-A C10
1901-B A2
1902-A D3
1902-B D2
1902-C D3
2200 F1
2201 F1
2202 H1
2203 H2
2902 B2
2903 B2
2906 A3
2909 B4
2910 B4
2912 E9
2913 E9
2915 D9
2916 D9
2917 D11
2919 E11
2920 D11
2923 E4
2924 E3
2925 F3
2926 D6
2927 E5
3200 G3
3201 G3
3250 G3
3280 A10
3281 B11
3282 C11
3900 A1
3901 A1
3902 A2
3903 A2
3905 C1
3906 D2
3907 D2
3908 F10
3909 D3
3910 C3
3911 C3
3913 C3
3915 B3
3916 B4
3918 B3
3919 B3
3920 A3
3921 C9
3922 D9
3923 D10
3924 C10
3925 E9
3928 F8
3929 F8
3930 F8
3932 F9
3935 E10
3936 E4
3937 E3
3938 E4
3939 E3
3940 F4
3941 F2
3942 E11
3944 D11
3945 D11
3946 C11
3970 D6
3971 D5
3972 E5
3991 B4
3992 C4
3993 C4
3994 C4
3995 D4
3996 E11
3997 F11
3999 E9
4911 D5
4912 H12
4913 E8
4914 A5
4922 B11
4934 A12
4936 A5
4937 A5
5200 F2
6200 H2
6201 G3
6202 H3
6203 G4
6204 G4
6205 H3
7280 B11
7900 C2
7901 F8
7905 D7

LSP (copper side overview)



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0020 C8	2468 A5	2923 F1	3511 D7	3736 D5	4522 D7
0030 A7	2469 A4	2924 F1	3512 C7	3737 E5	4610 D1
0035 A7	2480 C6	2925 F1	3513 B7	3738 D5	4611 D1
0040 D5	2488 C4	2926 E3	3514 C7	3739 E5	4701 F5
0041 G5	2489 C1	2927 F3	3515 B6	3740 E5	4702 G5
0045 F7	2490 A6	2941 G4	3516 C8	3741 D5	4707 F5
0317 B4	2491 D2	2942 G4	3518 C7	3742 F5	4708 F6
0324 A6	2492 D4	2943 F5	3519 C7	3743 E5	4709 F6
0325 A1	2495 D3	2944 G5	3520 C7	3744 D5	4710 F6
0390 D1	2498 B5	2946 G6	3521 A9	3745 E5	4722 F5
0391 A2	2499 C5	2951 G5	3522 C7	3752 F5	4723 G6
0392 A4	2501 C7	2952 F6	3523 D7	3753 F5	4724 F5
0393 C1	2502 C7	2953 F4	3524 C7	3754 F5	4736 F5
0395 B1	2503 D7	3101 C9	3525 C7	3756 G5	4737 F5
0735 F6	2505 A6	3102 D9	3526 B6	3757 F6	4910 E1
0736 F6	2507 B8	3103 D9	3527 D6	3758 F5	4911 F2
0737 F7	2508 A7	3104 C9	3528 E8	3762 F4	4912 E4
0738 F6	2509 A7	3105 D9	3529 E8	3763 G6	4913 F1
0739 F5	2510 B6	3106 E9	3530 D7	3764 F6	4914 E1
0933 F1	2512 E6	3107 D9	3531 C7	3765 G5	4916 G1
0934 E1	2513 D7	3108 C9	3533 D6	3770 F5	4917 F1
0935 F1	2514 D7	3110 C8	3535 E6	3773 F5	4919 E4
0936 E4	2515 C6	3113 E9	3536 E6	3781 F6	4920 E1
0937 G2	2516 B7	3114 E9	3537 E6	3784 F7	4922 G3
0938 F1	2517 A6	3117 D9	3538 E6	3789 F6	4923 E5
0939 F2	2518 C7	3118 C9	3539 E6	3790 G4	4924 E5
0940 E2	2519 E7	3120 E9	3540 D6	3792 G5	4925 E5
0942 G3	2520 C7	3123 E9	3541 E6	3794 F5	4926 F5
0943 G1	2521 A6	3124 E9	3542 B6	3795 F5	4927 F5
0945 E10	2523 C6	3125 C10	3543 C7	3796 F5	4928 F5
0946 G2	2528 E8	3126 C10	3544 B7	3798 G5	4929 G1
0947 A10	2530 D7	3127 C9	3600 C1	3900 D1	4932 E1
0948 G2	2531 D6	3200 G1	3601 C1	3901 D1	4934 G3
1001 A8	2535 E6	3201 G1	3602 B1	3902 D1	4935 E1
1002 D8	2536 E7	3237 E9	3603 B1	3903 D1	4936 E1
1003 A6	2537 A8	3250 G1	3605 A1	3905 E1	4937 E1
1200 G1	2538 B7	3280 G3	3606 B1	3906 E1	5101 E8
1201 F1	2600 C1	3281 G3	3607 A1	3907 E1	5102 D9
1205 E3	2601 C1	3282 G3	3608 A1	3908 F1	5103 E8
1501 B9	2602 B1	3401 B4	3609 A1	3909 F1	5104 D8
1503 B7	2603 A1	3402 D3	3610 A1	3910 E1	5105 C8
1901 E1	2604 A1	3403 D3	3611 B1	3911 E1	5110 E7
1902 F1	2605 C1	3404 D3	3612 B1	3913 E1	5115 E7
2101 D9	2610 B1	3406 D4	3613 B1	3915 E1	5200 G2
2102 D9	2620 A1	3407 D4	3614 B1	3916 E1	5400 A6
2103 D9	2621 A1	3409 C2	3615 B1	3918 E1	5401 B4
2104 E8	2622 A1	3410 D4	3616 B1	3919 E1	5410 D2
2105 C9	2624 A1	3411 D3	3617 C1	3920 D1	5411 C3
2106 C9	2625 A1	3414 D4	3618 B1	3921 D2	5421 B4
2107 E9	2627 A1	3415 D4	3619 C1	3922 E2	5422 C6
2108 C9	2629 A1	3416 D4	3620 B1	3923 D1	5423 C5
2109 E9	2640 B1	3417 C4	3621 B1	3924 D1	5424 C5
2110 C9	2642 C2	3418 C6	3622 B1	3925 F1	5425 C5
2111 C9	2653 A1	3423 C4	3623 A1	3928 F1	5426 C4
2113 E8	2704 G4	3425 C5	3624 A1	3929 F1	5430 B3
2114 B9	2710 F5	3426 C5	3625 A1	3930 F1	5460 A3
2200 F1	2711 F4	3431 B4	3626 A1	3932 F1	5461 A3
2201 G1	2712 F4	3439 C1	3627 B1	3935 F1	5462 C2
2202 G1	2730 D4	3440 C1	3629 A1	3936 F1	5463 C2
2203 G1	2731 E4	3441 C1	3630 D1	3937 F1	5464 C3
2400 B5	2732 E6	3442 C1	3631 D1	3938 F1	5465 C3
2401 B4	2733 E6	3443 C1	3632 C1	3939 F1	5466 A5
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2412 D3	2735 E5	3445 C1	3640 B1	3941 F1	5503 B8
2413 D3	2736 E5	3446 C1	3641 B1	3942 E1	5504 B8
2414 D3	2737 E5	3447 C1	3642 B1	3944 E1	5505 C7
2415 D4	2738 D5	3450 A6	3643 B1	3945 E1	5506 D7
2416 D3	2739 E5	3451 A5	3644 A1	3946 D1	5510 A6
2417 D4	2756 F6	3460 A4	3645 C2	3970 F3	5620 A1
2418 C3	2758 F5	3461 A4	3652 C3	3971 F3	6103 D9
2419 C5	2759 G6	3462 C2	3653 A1	3972 F3	6105 D9
2420 C3	2760 F6	3463 C1	3701 G4	3991 E1	6106 C9
2421 B6	2761 F3	3464 C3	3702 G3	3992 E1	6107 E8
2422 B6	2762 G6	3465 C2	3703 G6	3993 E1	6108 B9
2423 B5	2763 G6	3466 A5	3704 G5	3994 E1	6109 B9
2425 C4	2765 G4	3467 A5	3708 G5	3995 E2	6111 E8
2426 C4	2766 F7	3468 A4	3710 G4	3996 E2	6120 E9
2429 C5	2767 G4	3469 A5	3711 G4	3997 E2	6121 E9
2430 C6	2768 G6	3475 A5	3712 F4	3998 E10	6122 E9
2431 B4	2774 F6	3481 D6	3713 F4	3999 F2	6200 G1
2432 B5	2775 F7	3483 D2	3714 G4	4102 E9	6201 G1
2433 B4	2776 F7	3484 D2	3715 G4	4103 E9	6202 G1
2434 B5	2782 F4	3485 D2	3716 G4	4401 C1	6203 G1
2435 C4	2783 F6	3486 D2	3717 G4	4402 C1	6204 G1
2443 C1	2784 G5	3487 D2	3718 G5	4403 A1	6205 G1
2444 D1	2785 G5	3488 D1	3719 G6	4404 C6	6405 C2
2445 D1	2786 G5	3489 B1	3721 F4	4405 D2	6406 D4
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2447 C1	2902 D1	3491 D1	3723 F4	4407 A1	6408 D4
2450 A2	2903 D1	3495 C5	3724 F4	4408 B1	6421 D4
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2461 A4	2912 F1	3502 A7	3728 F4	4441 D1	6441 D1
2462 C1	2913 F1	3503 A9	3730 D5	4442 D3	6442 A1
2463 C1	2915 D1	3504 C7	3731 E5	4443 D3	6460 A4
2464 C2	2916 D1	3507 D6	3732 E5	4444 D3	6461 A4
2465 C2	2917 D1	3508 C7	3733 E5	4482 D2	6462 C1
2466 A6	2919 E1	3509 B9	3734 E5	4483 D2	6463 C1

6464 C2	9202 F2	9929 F3
6465 C2	9203 F5	9930 E1
6466 A5	9204 F6	9931 G1
6468 A4	9205 F6	9932 E2
6480 C5	9206 F5	9933 E3
6481 D6	9207 E4	9934 F3
6482 D2	9208 G2	9935 F2
6483 C2	9209 E4	9936 E4
6499 C5	9210 G3	9943 E3
6501 A7	9211 G3	9944 E4
6502 A7	9212 G2	9945 E5
6503 A7	9213 E1	9946 F3
6504 A6	9214 E5	9947 E5
6505 C6	9215 E4	9948 D4
6506 C7	9216 F2	9950 D4
6507 E7	9217 E2	9951 D5
6508 C7	9218 E1	9952 D4
6510 B6	9220 E1	9957 F3
6511 D8	9221 G2	9958 E5
6512 D8	9222 F6	9960 E3
6514 D6	9223 F4	9961 F3
6515 B8	9224 F6	9962 F3
6516 D7	9225 D1	9963 F5
6517 D6	9226 F1	9964 F5
6518 C7	9227 F1	9965 F2
6520 E7	9228 F1	9966 F5
6521 E6	9229 G1	9967 D5
6522 E6	9230 E2	9968 D6
6600 C1	9231 E2	9969 F3
6616 B1	9401 B4	9970 F2
6619 A1	9402 B1	9971 F2
6620 A1	9403 B1	9972 G1
6621 A1	9404 B1	9976 D1
6622 A1	9408 C2	9980 E2
6623 B2	9412 C3	9981 F1
6730 G4	9414 C3	9982 F1
6731 G4	9418 B1	9983 F1
7100 C9	9421 C2	9984 F2
7101 C9	9423 C4	9985 G2
7102 D8	9424 D1	9987 F2
7103 E9	9425 C5	9988 F2
7104 E9	9426 C4	9989 E3
7280 G3	9428 C2	9990 E2
7407 D3	9429 C4	9991 F4
7408 D3	9430 C3	9992 F4
7409 D4	9431 A1	9993 F2
7421 D3	9466 A5	9994 F2
7440 C1	9480 C5	9995 F2
7441 C1	9501 B7	9996 F3
7442 C1	9502 B7	9997 G2
7480 D5	9503 B7	9998 G3
7481 D2	9504 B7	9999 F4
7482 D2	9505 D8	
7483 D2	9511 C7	
7502 C8	9512 C7	
7504 C7	9513 C7	
7505 C8	9514 C8	
7506 D8	9515 E6	
7510 E6	9517 E7	
7511 E6	9518 C7	
7528 E7	9519 C8	
7529 D7	9520 E6	
7600 C1	9523 D7	
7602 B1	9524 D7	
7603 B1	9525 C7	
7605 C1	9526 A7	
7606 C1	9620 A1	
7610 D1	9622 A1	
7611 D1	9623 B2	
7620 A1	9624 B3	
7640 B1	9705 G7	
7641 C2	9707 G4	
7652 B6	9712 F5	
7701 G6	9713 G4	
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7711 F5	9718 G4	
7715 F4	9720 G3	
7720 D5	9721 G6	
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7722 D5	9723 F5	
7723 E5	9906 D6	
7724 D5	9907 E3	
7725 E5	9908 E3	
7730 G4	9909 E2	
7731 G4	9910 E2	
7732 G4	9911 E2	
7733 G6	9912 E2	
7740 G5	9913 E2	
7750 G4	9914 E3	
7900 E1	9915 E3	
7901 F1	9916 E3	
7905 E3	9917 E3	
7906 F2	9918 E3	
7907 F3	9919 E3	
9001 C9	9922 E2	
9102 D9	9925 F2	
9110 E7	9926 F2	
9115 E7	9927 F3	
9201 G3	9928 F3	

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030300

Part 2

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180200

Part 4

CL96532156_086.pdf
180200

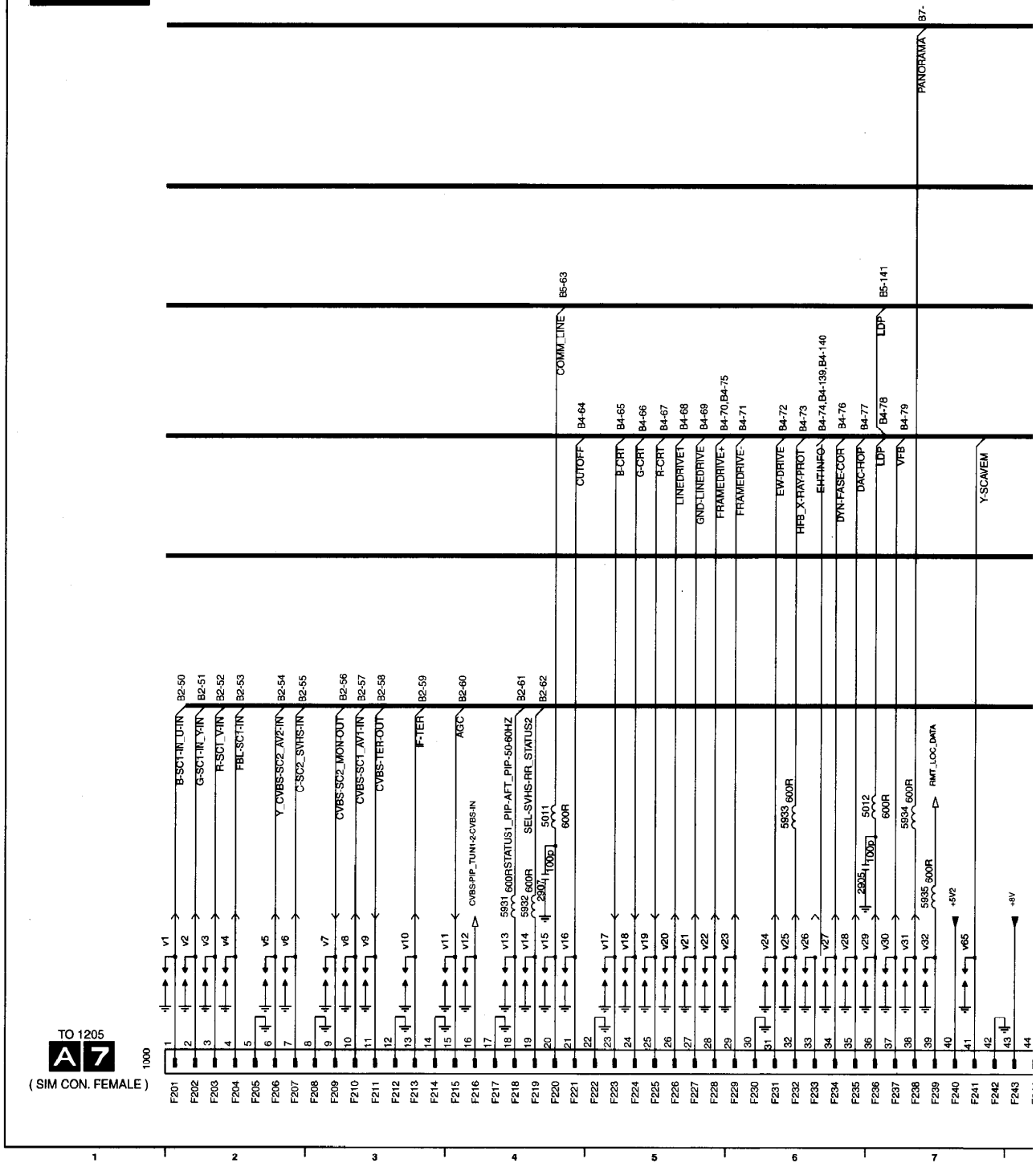
CL96532156_073.eps
030300

Sim connector (male)

v5 G2	v9 G3	v13 G4	v17 G5	v21 G5	v25 G6	v29 G7	v33 G8	v37 G9	v41 G9	v45 G10	v49 G11	v53 G11	v57 G12	v61 G12	v65 G7
v6 G2	v10 G3	v14 G4	v18 G5	v22 G5	v26 G6	v30 G7	v34 G8	v38 G9	v42 G9	v46 G10	v50 G11	v54 G11	v58 G12	v62 G13	0010 G14
v7 G3	v11 G4	v15 G4	v19 G5	v23 G6	v27 G6	v31 G7	v35 G8	v39 G9	v43 G10	v47 G10	v51 G11	v55 G11	v59 G12	v63 G13	1000 H1
v8 G3	v12 G4	v16 G4	v20 G5	v24 G6	v28 G6	v32 G7	v36 G8	v40 G9	v44 G10	v48 G10	v52 G11	v56 G12	v60 G12	v64 G13	2900 G12

1 2 3 4 5 6 7

B 1 SIM CONNECTOR (MALE)



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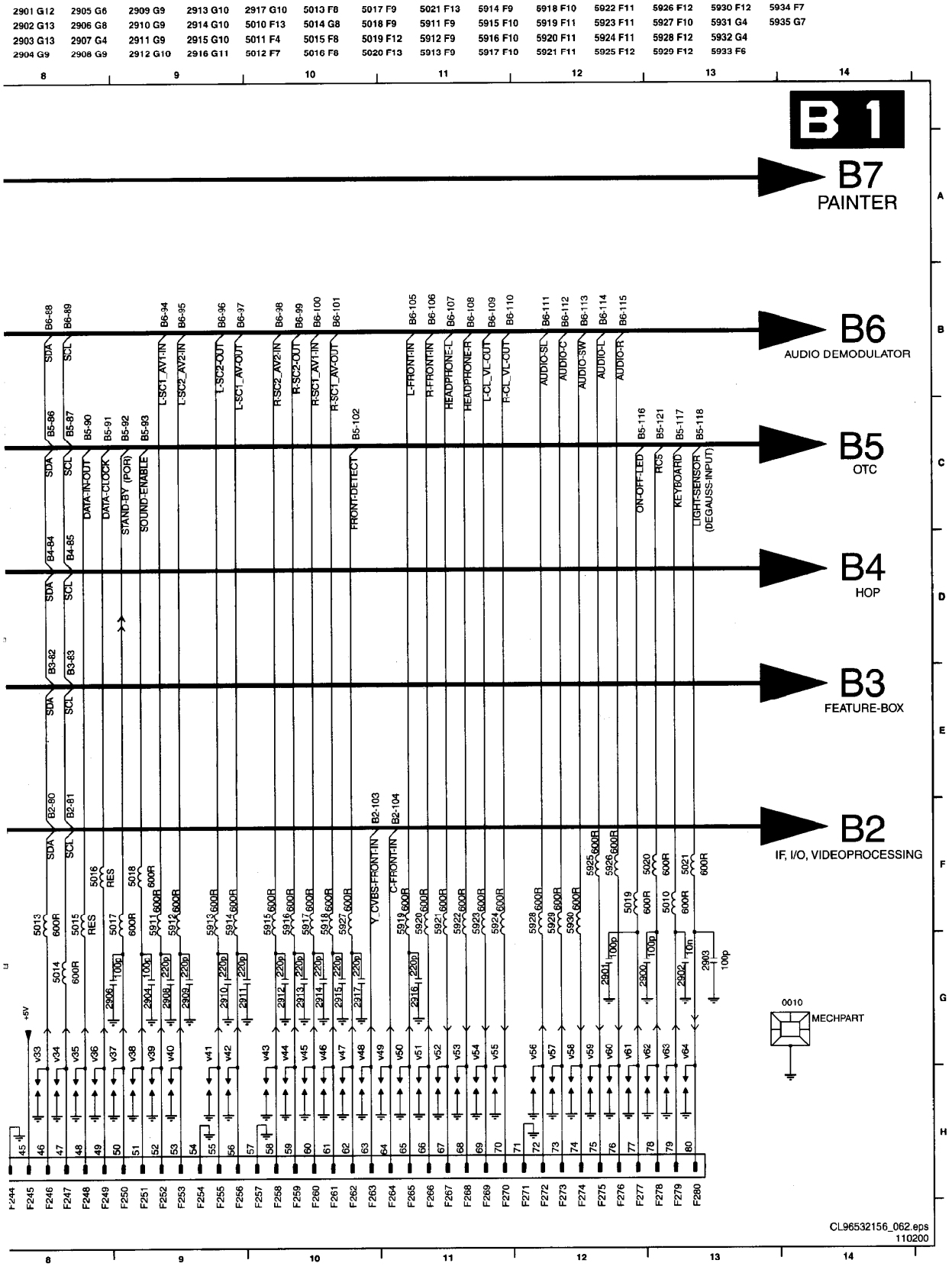
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2904 G9
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2912 G10
2913 G10
2914 G10
2915 G10
2916 G11
2917 G10
5010 F13
5011 F4
5012 F7
5013 F8
5014 G8
5015 F8
5016 F8
5017 F9
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5917 F10
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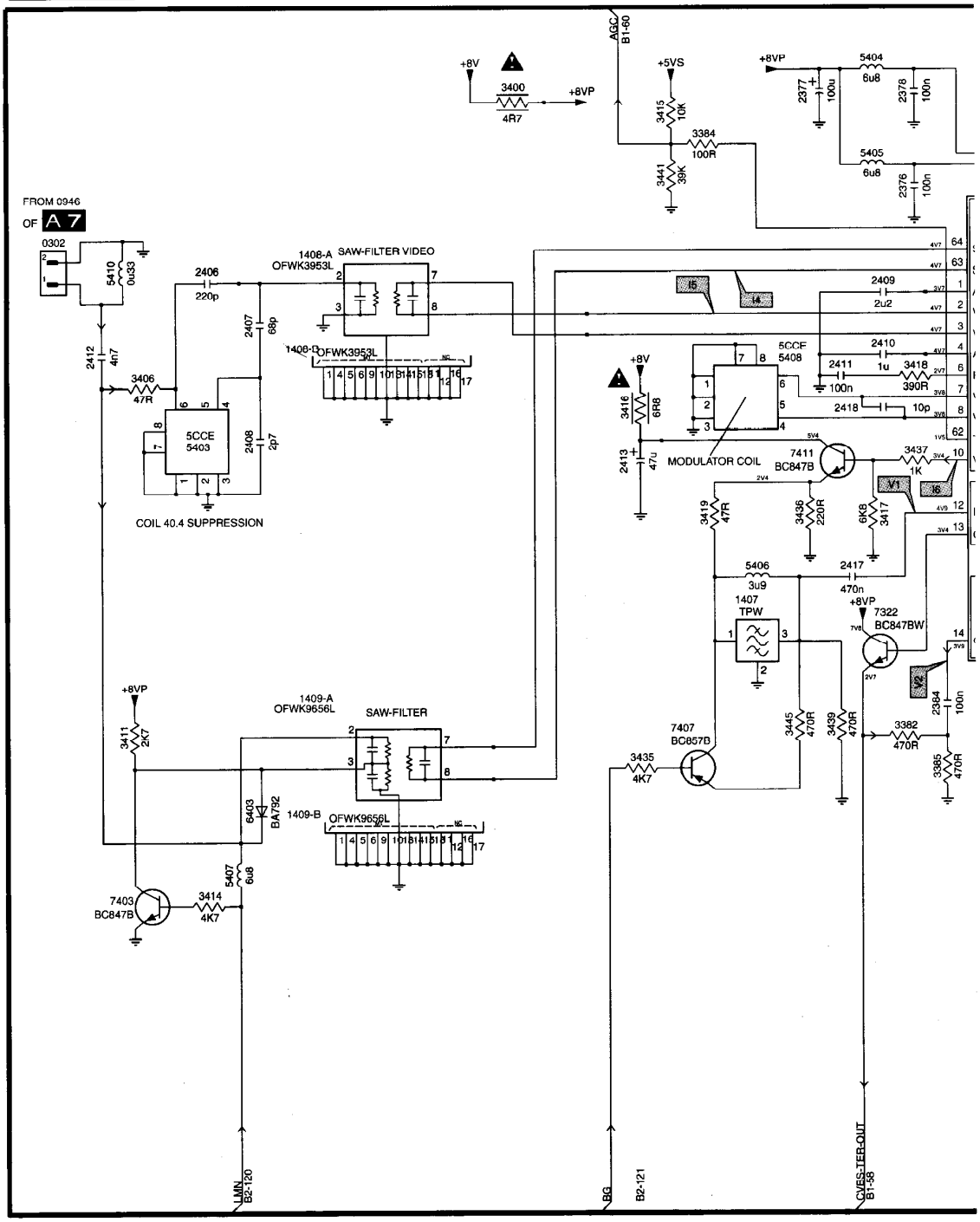
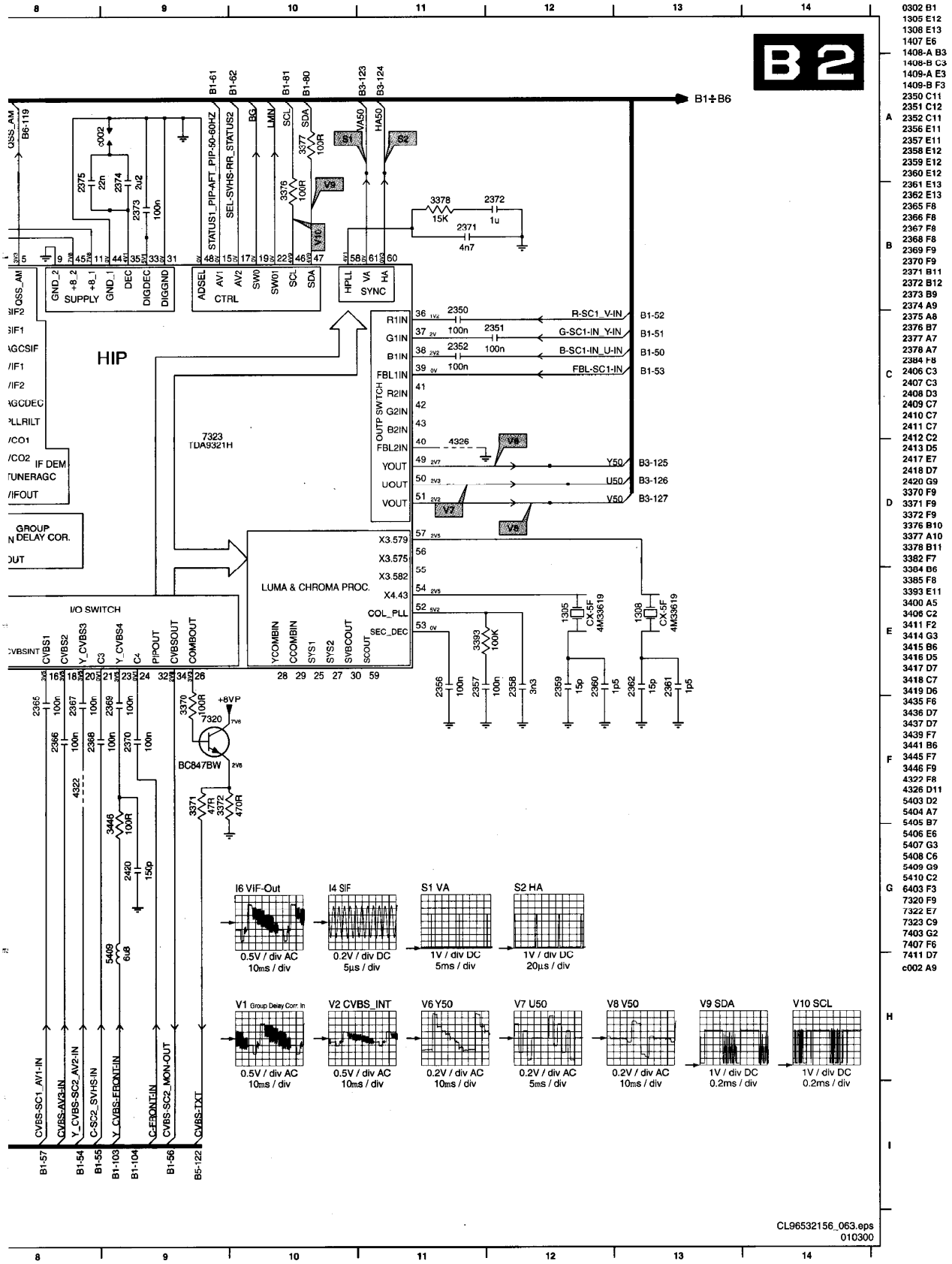
5921 F11
5922 F11
5923 F11
5924 F11
5925 F12
5926 F12
5927 F10
5928 F12
5929 F12
5930 F12
5931 G4
5932 G4
5933 F6
5934 F7
5935 G7
B 1
B7
PAINTER
B6
AUDIO DEMODULATOR
B5
OTC
B4
HOP
B3
FEATURE-BOX
B2
IF, I/O, VIDEOPROCESSING
0010
MECHPART
CL96532156_062.eps
110200

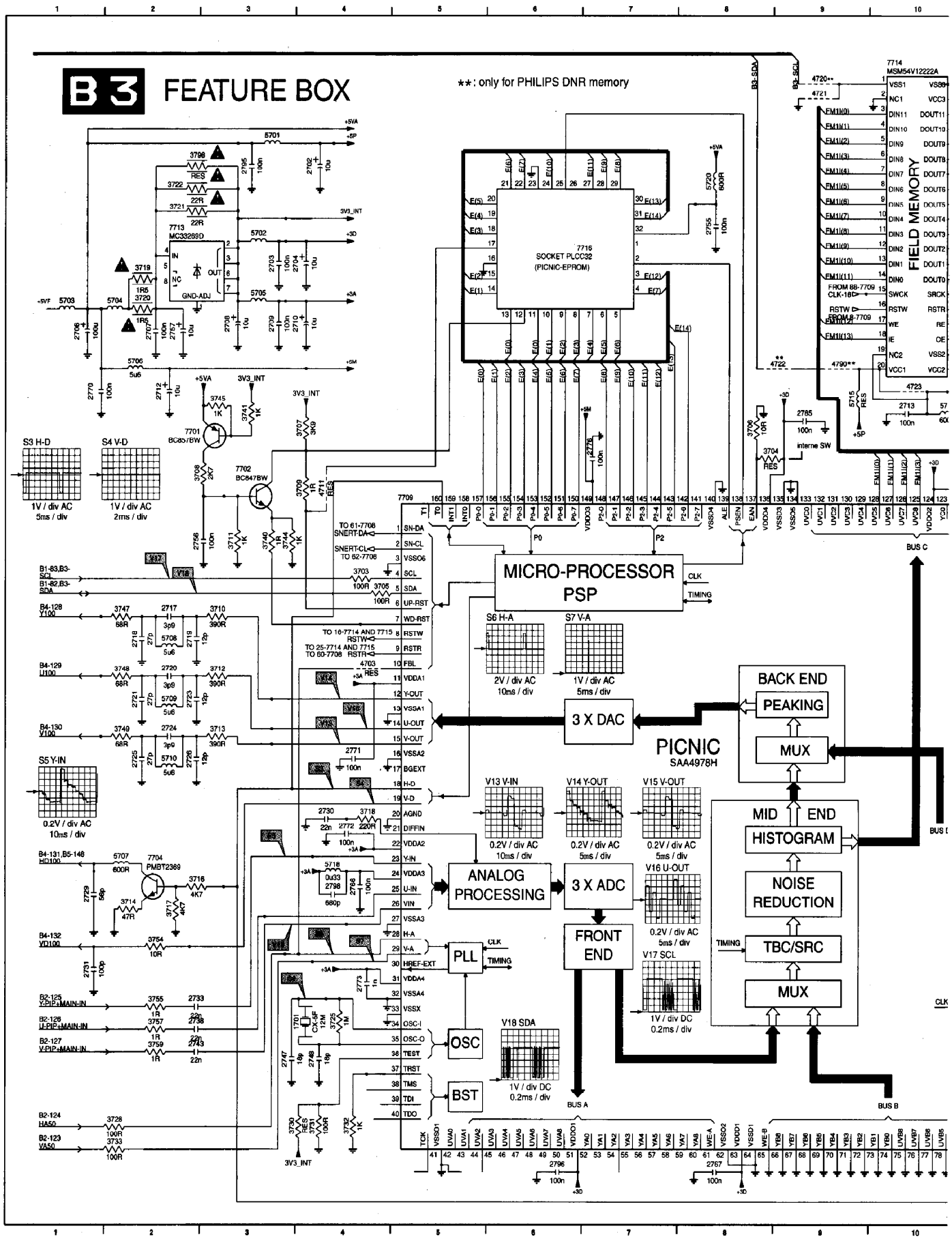
IF, I/O videoprocessing

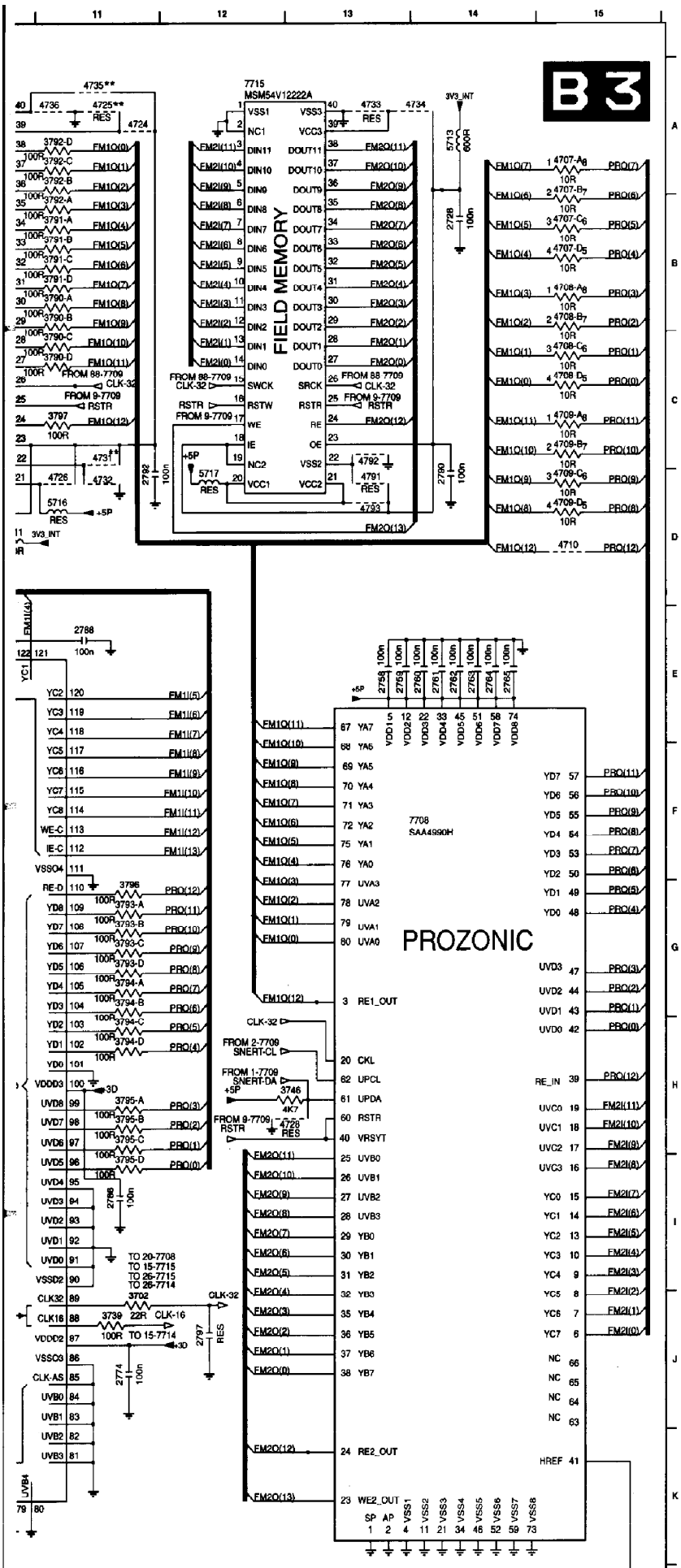
B2 IF,I/O VIDEOPROCESSING





Feature box


B3 FEATURE BOX
**: only for PHILIPS DNR memory
FIELD MEMORY
MICRO-PROCESSOR PSP
PICNIC SAA4978H
BACK END
PEAKING
MUX
3 X DAC
MID END
HISTOGRAM
NOISE REDUCTION
TBC/SRC
MUX
ANALOG PROCESSING
3 X ADC
FRONT END
PLL
OSC
BST
SOCKET PLCC32 (PICNIC-EPROM)
MC33269D
BC847BW
BC857BW
PMBT2369
S3 H-D
S4 V-D
S5 Y-IN
S6 H-A
S7 V-A
V13 V-IN
V14 Y-OUT
V15 V-OUT
V16 U-OUT
V17 SCL
V18 SDA
BUS A
BUS B
BUS C



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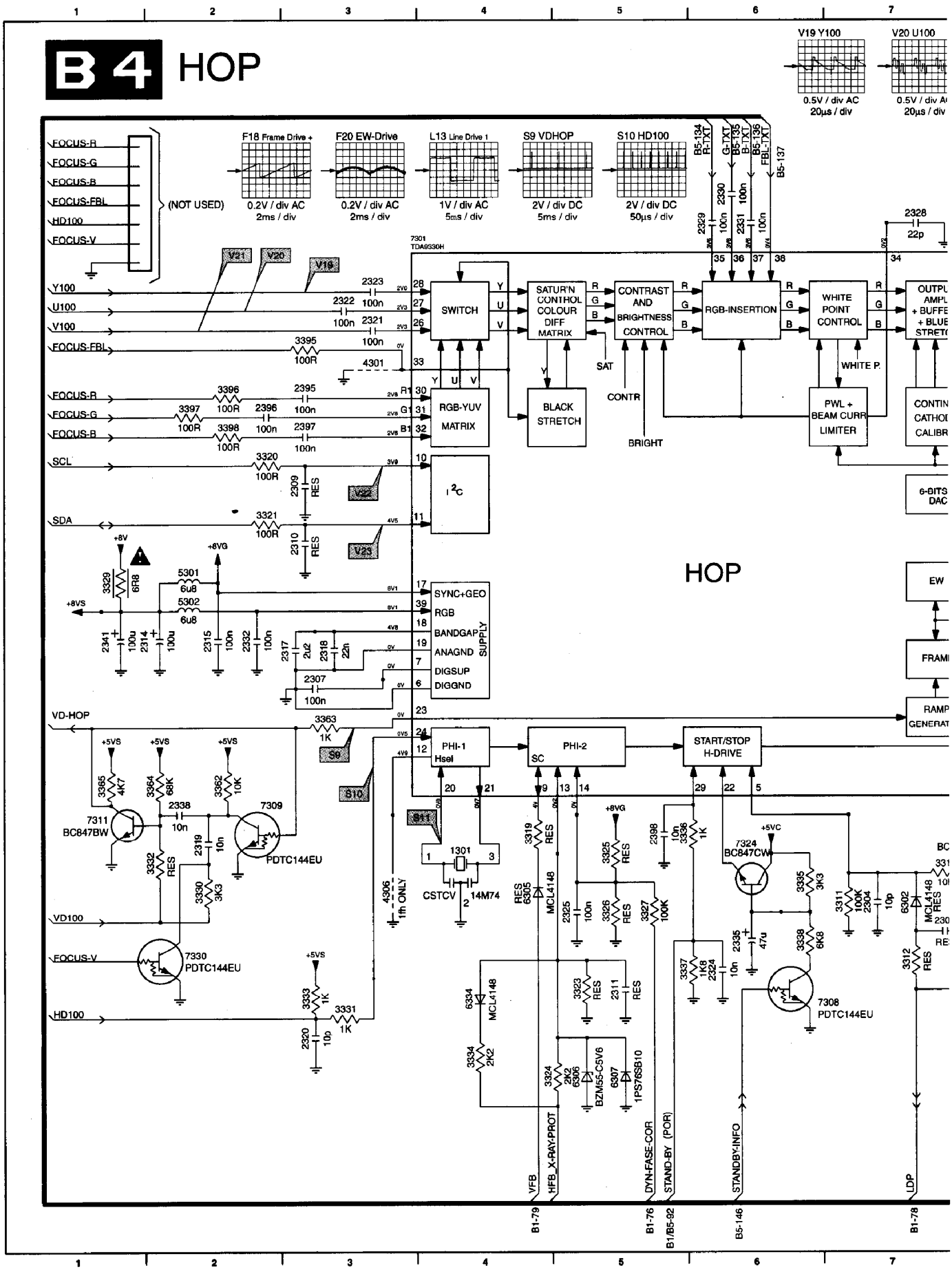
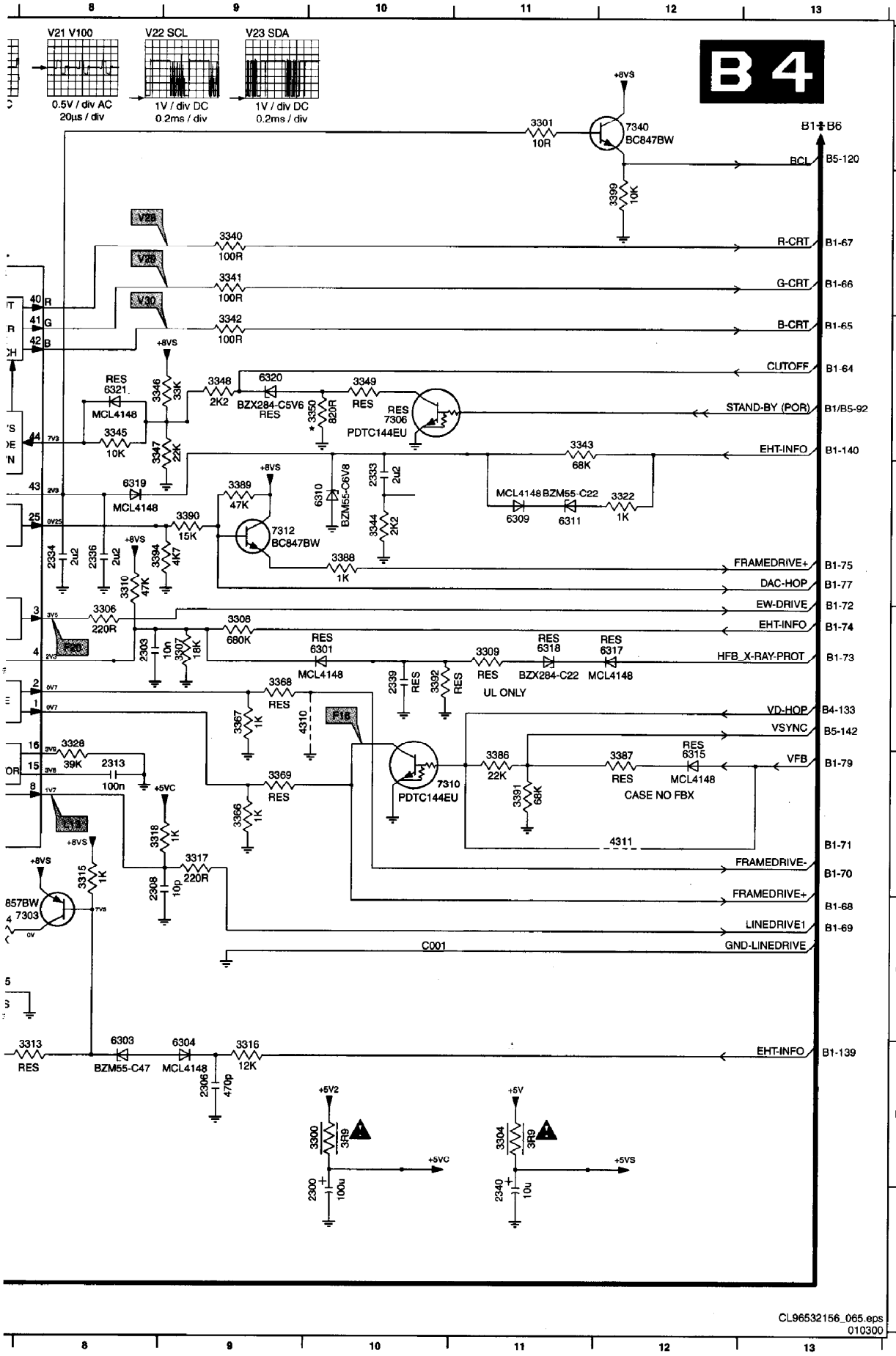
2707 C2	3794-B G11
2708 C3	3794-C H11
2709 C3	3794-D H11
2710 C4	3795-A H11
2712 D2	3795-B H11
2713 D10	3795-C H11
2717 F2	3795-D I11
2718 F2	3796 G11
2719 F2	3797 C11
2720 F2	3798 B2
2721 G2	4703 F4
2723 G2	4707-A A15
2724 G2	4707-B A15
2725 G2	4707-C B15
2726 G2	4707-D B15
2728 B14	4708-A B15
2729 I1	4708-B B15
2730 H4	4708-C C15
2731 I1	4708-D C15
2733 J2	4709-A C15
2738 J2	4709-B C15
2743 J2	4709-C D15
2747 J3	4709-D D15
2748 J4	4710 D15
2755 B8	4711 E4
2756 E2	4720 A9
2757 C2	4721 A9
2758 E13	4722 D9
2759 E13	4723 D10
2760 E14	4724 A11
2761 E14	4725 A11
2762 E14	4726 D11
2763 E14	4728 H13
2764 E14	4731 C11
2765 E14	4732 D11
2766 I4	4733 A13
2767 K8	4734 A14
2770 D1	4735 A11
2771 G4	4736 A11
2772 H4	4790 D9
2773 I4	4791 D13
2774 J11	4792 C13
2776 D7	4793 D13
2785 D9	5701 A3
2786 I11	5702 B3
2788 E11	5703 C1
2790 D14	5704 C2
2792 D11	5705 C3
2795 B3	5706 D2
2796 K6	5707 H2
2797 J12	5708 F2
2798 I4	5709 G2
3702 J11	5710 G2
3703 F4	5711 D10
3704 D8	5713 A14
3705 F4	5715 D9
3706 D8	5716 D11
3707 D4	5717 D12
3708 E2	5718 H4
3709 E4	5720 B8
3710 F3	7701 D2
3711 E3	7702 E3
3712 F3	7704 H2
3713 G3	7708 F13
3714 I2	7709 E5
3716 H2	7713 B2
3717 I2	7714 A10
3718 H4	7715 A12
3719 C2	7716 B7
3720 C2	
3721 B2	
3722 B2	
3725 J4	
3728 K2	
3730 K3	
3731 K4	
3732 K4	
3733 K2	
3739 J11	
3740 E3	
3741 D3	
3744 E3	
3745 D3	
3746 H12	
3747 F2	
3748 F2	
3749 G2	
3754 I2	
3755 J2	
3757 J2	
3759 J2	
3790-A B11	
3790-B B11	
3790-C C11	
3790-D C11	
3791-A B11	
3791-B B11	
3791-C B11	
3791-D B11	
3792-A B11	
3792-B A11	
3792-C A11	
3792-D A11	

Diversity Small Signal Panel (B3)

Item	100HZ INCR ST	DS VRT DLB	100HZ DLB
2728	-	100N	-
2758	-	100N	-
2759	-	100N	-
2760	-	100N	-
2761	-	100N	-
2762	-	100N	-
2763	-	100N	-
2764	-	100N	-
2765	-	100N	-
2790	-	100N	-
3793	10R	100R	10R
3794	10R	100R	10R
3795	10R	100R	10R
3796	10R	100R	10R
4707	10R	-	10R
4708	10R	-	10R
4709	10R	-	10R
4710	JUMP	-	JUMP
4734	-	JUMP	-
4792	-	JUMP	-
4793	-	JUMP	-
5713	-	FXDIND	-
7708	-	SAA4990H	-
7715	-	MSM54V12222A-30JS	-

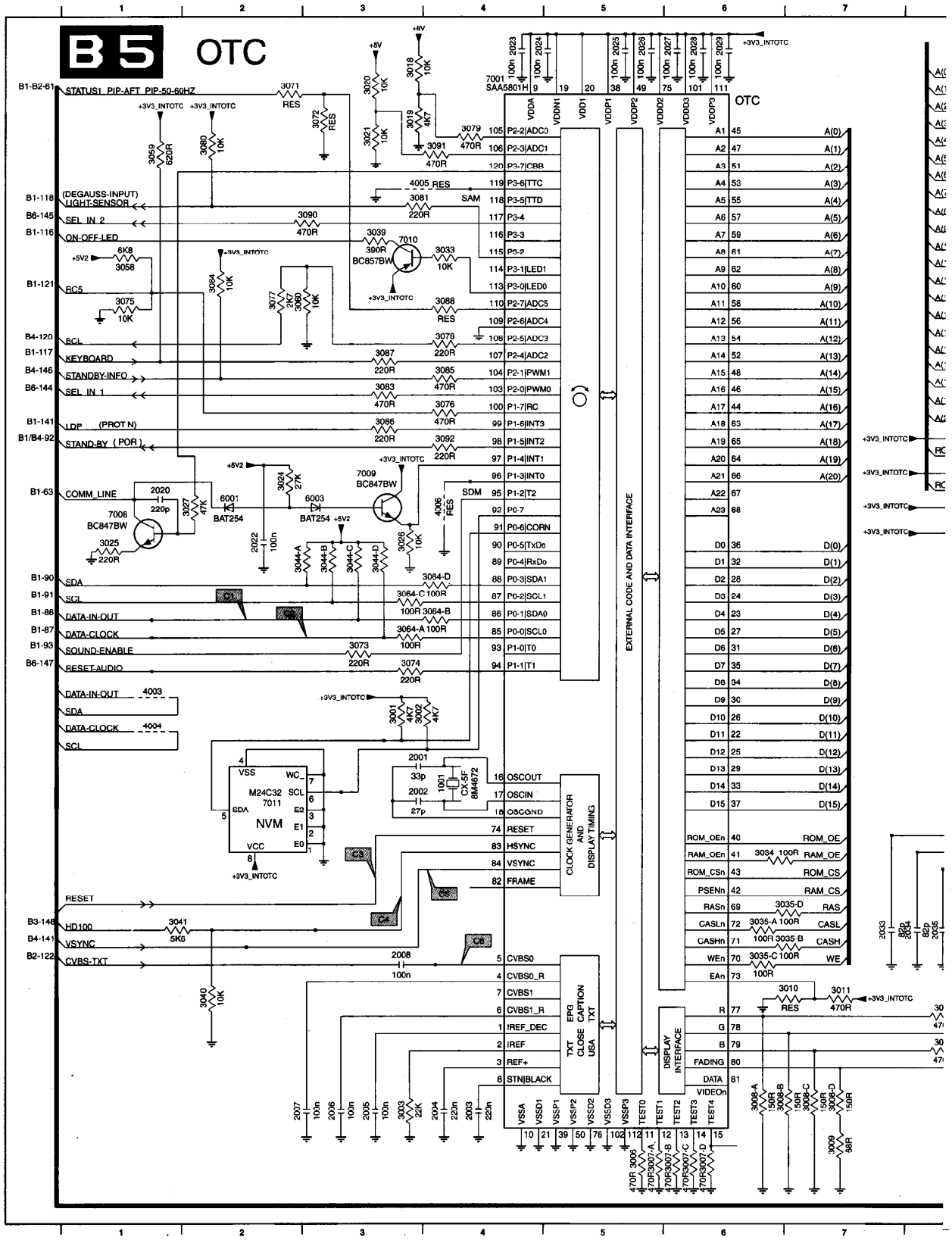
HOP

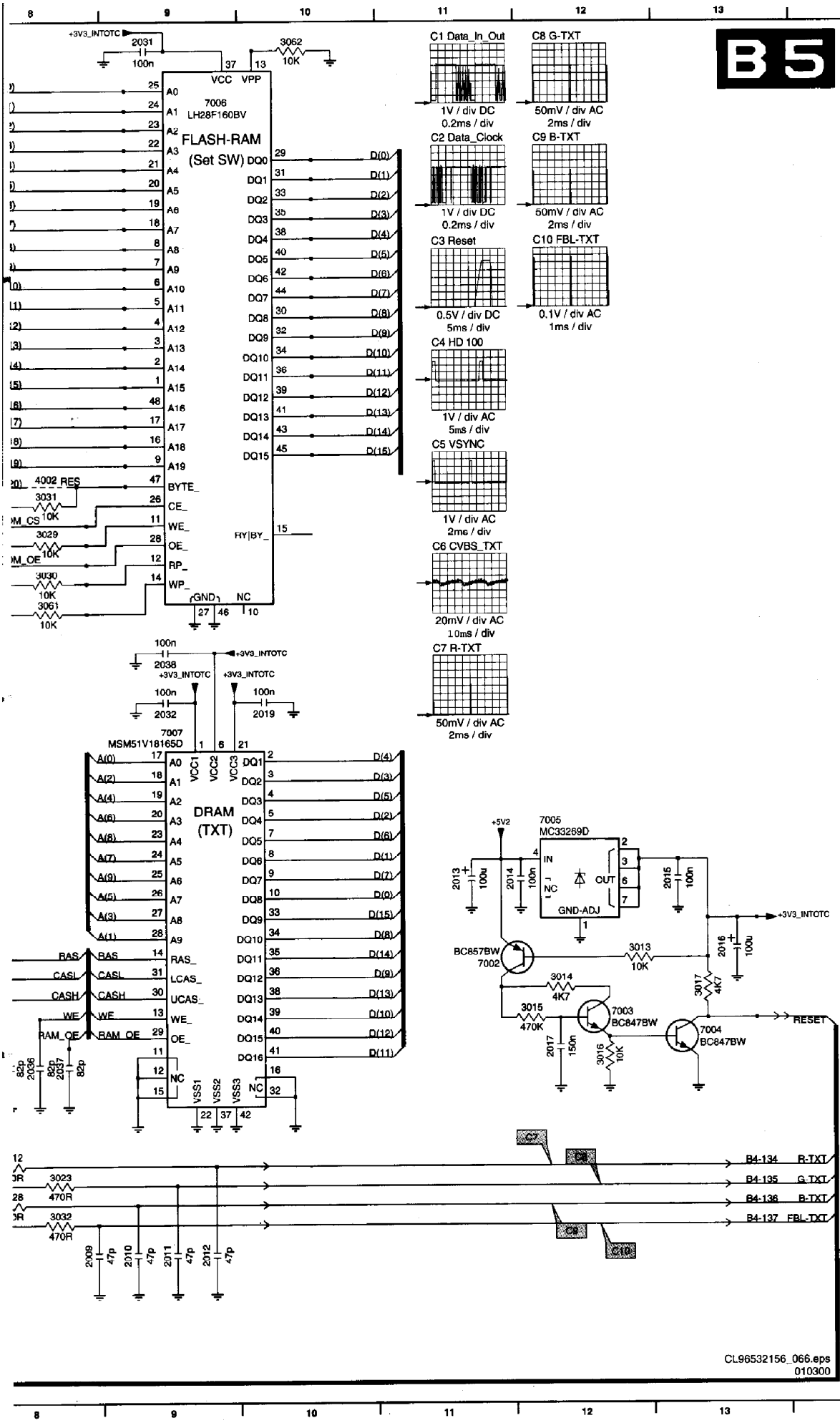

B 4 HOP
V19 Y100
V20 U100
0.5V / div AC
20µs / div
F18 Frame Drive +
0.2V / div AC
2ms / div
F20 EW-Drive
0.2V / div AC
2ms / div
L13 Line Drive 1
1V / div AC
5ms / div
S9 VDHOP
2V / div DC
5ms / div
S10 HD100
2V / div DC
50µs / div
FOCUS-R
FOCUS-G
FOCUS-B
FOCUS-FBL
HD100
FOCUS-V
(NOT USED)
7301
TDA9330H
SWITCH
SATUR'N CONTROL COLOUR DIFF MATRIX
CONTRAST AND BRIGHTNESS CONTROL
RGB-INSERTION
WHITE POINT CONTROL
RGB-YUV MATRIX
BLACK STRETCH
PWL + BEAM CURR LIMITER
I²C
SYNC+GEO
RGB
BANDGAP
ANAGND
DIGSUP
DIGGND
SUPPLY
PHI-1
Hsel
PHI-2
SC
START/STOP H-DRIVE
HOP
VD-HOP
VD100
HD100
7311 BC847BW
7309 PDTC144EU
7330 PDTC144EU
7324 BC847CW
7308 PDTC144EU
CSTCV 14M74
MCL4148
BZM55-C5V6
1PS76SB10
VFB
HFB_X-RAY-PROT
DYN-FASE-COR
STAND-BY (POR)
STANDBY-INFO
LDP
B1-79
B1-76
B1/B5-92
B5-146
B1-78



	1301 G4	3349 C10
	2300 I10	3350 C10
	2303 E8	3362 F2
	2304 G7	3363 F3
	2305 G7	3364 F2
A	2306 H9	3365 F1
	2307 E3	3366 F9
	2308 F8	3367 E9
	2309 D3	3368 E9
	2310 D3	3369 F9
	2311 H5	3386 F11
	2313 F8	3387 F12
	2314 E2	3388 D10
	2315 E2	3389 D9
	2317 E3	3390 D9
B	2318 E3	3391 F11
	2319 G2	3392 E10
	2320 H3	3394 D8
	2321 C3	3395 C3
	2322 C3	3396 C2
	2323 B3	3397 C2
	2324 G6	3398 C2
	2325 G5	3399 B12
	2328 B7	4301 C3
C	2329 B6	4306 G3
	2330 B6	4310 E10
	2331 B6	4311 F12
	2332 E2	5301 E2
	2333 D10	5302 E2
	2334 D8	6301 E10
	2335 G6	6302 G7
	2336 D8	6303 H8
	2338 F2	6304 H9
D	2339 E10	6305 G4
	2340 I11	6306 H5
	2341 E1	6307 H5
	2395 C3	6309 D11
	2396 C2	6310 D10
	2397 C3	6311 D11
	2398 F5	6315 F12
	3300 H10	6317 E12
	3301 A11	6318 E11
	3304 H11	6319 D8
E	3306 E8	6320 C9
	3307 E9	6321 C8
	3308 E9	6334 H4
	3309 E11	7301 B3
	3310 D8	7303 G8
	3311 G7	7306 C10
	3312 G7	7308 H6
	3313 H8	7309 F3
	3314 G7	7310 F11
F	3315 F8	7311 F1
	3316 H9	7312 D9
	3317 F9	7324 G6
	3318 F8	7330 G2
	3319 F4	7340 A12
	3320 D2	C001 G10
	3321 D2	
	3322 D12	
	3323 H5	
G	3324 H4	
	3325 G5	
	3326 G5	
	3327 G5	
	3328 E8	
	3329 E1	
	3330 G2	
	3331 H3	
	3332 G2	
	3333 H3	
H	3334 H4	
	3335 G6	
	3336 F5	
	3337 G5	
	3338 G6	
	3340 B9	
	3341 B9	
	3342 C9	
	3343 C11	
I	3344 D10	
	3345 C8	
	3346 C8	
	3347 C8	
	3348 C9	

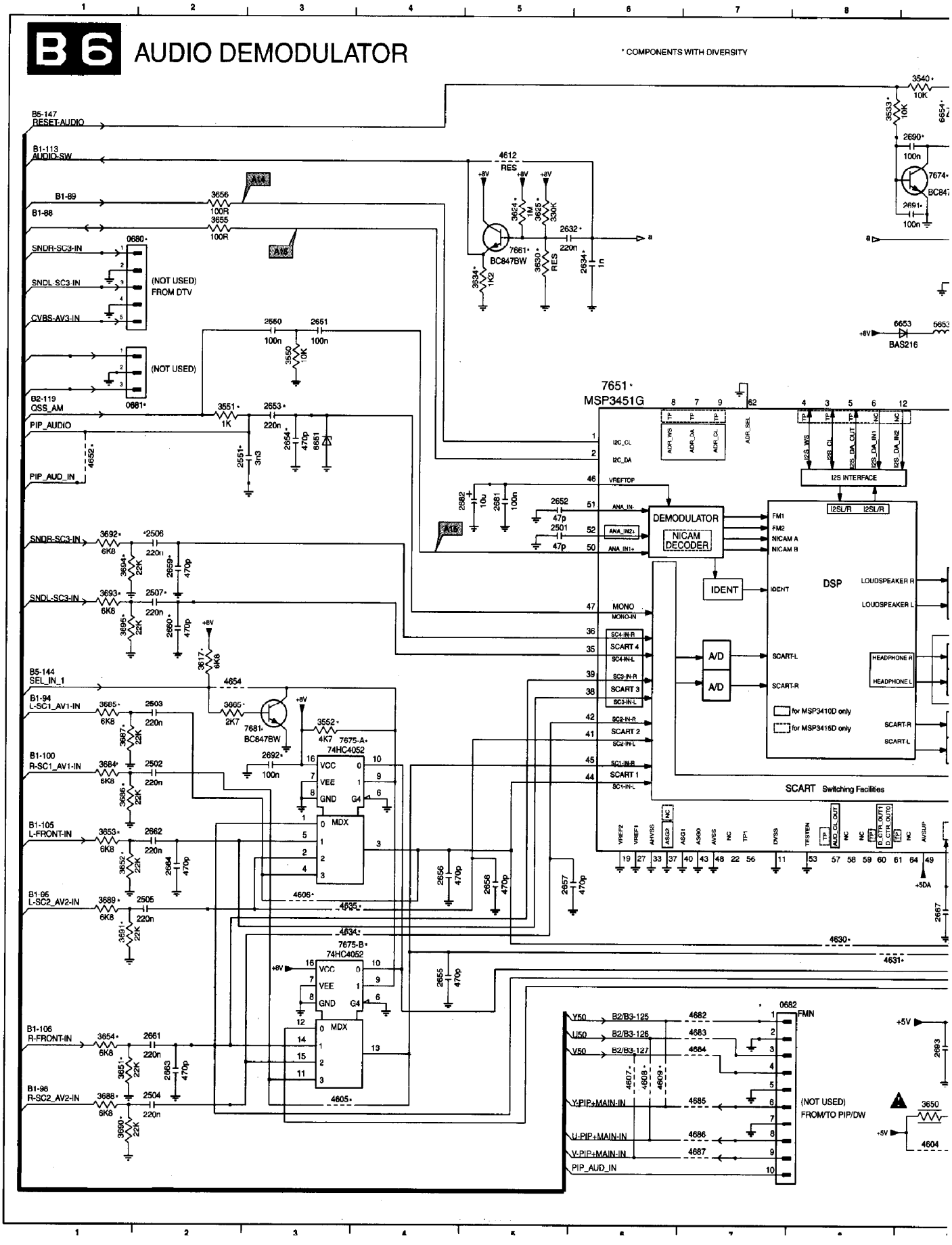
OTC

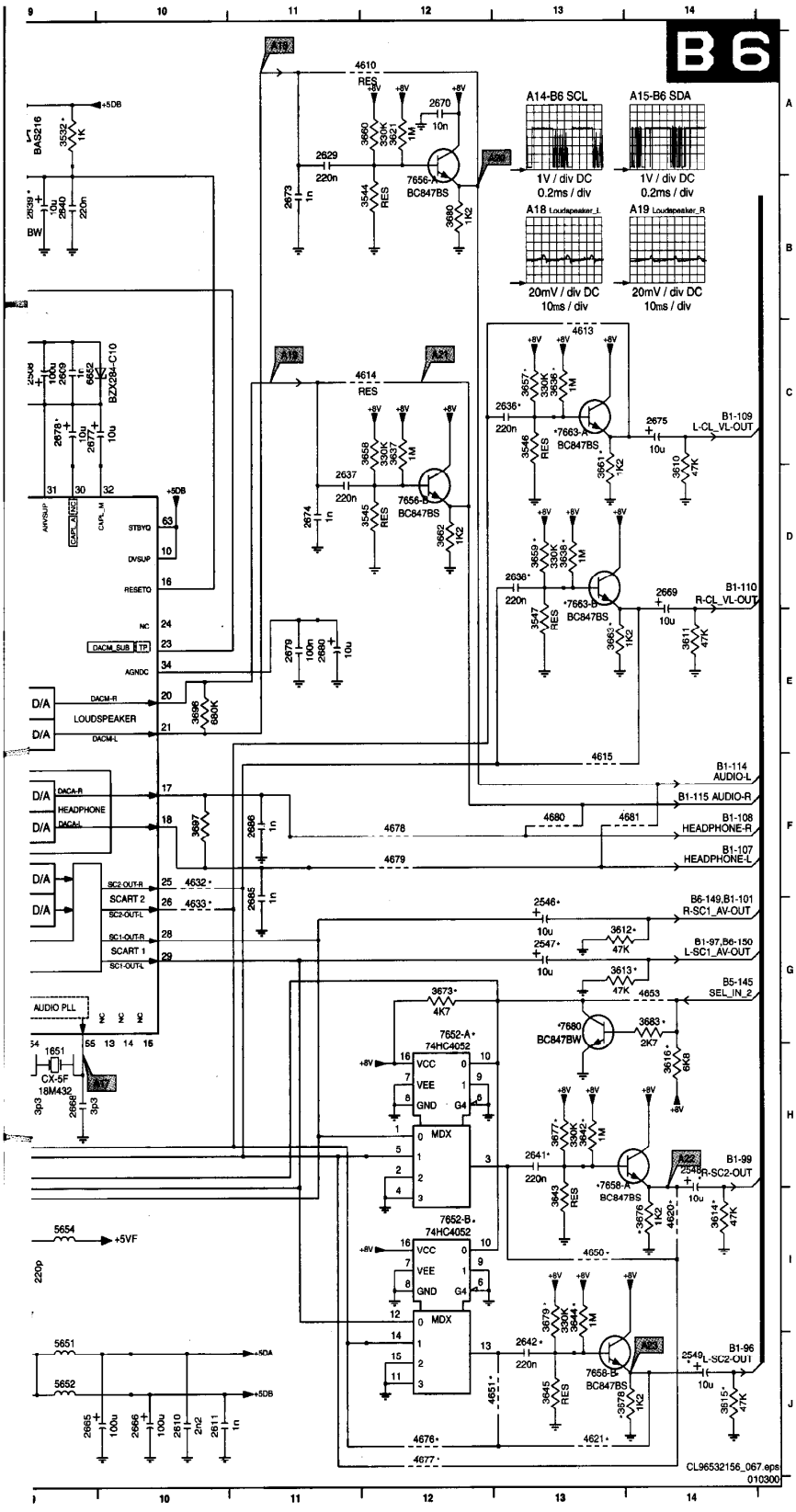

B5
OTC
STATUS1_PIP-AFT_PIP-50-60HZ
(DEGAUSS-INPUT)
LIGHT-SENSOR
SEL_IN_2
ON-OFF-LED
RC5
SCL
KEYBOARD
STANDBY-INFO
SEL_IN_1
LDP (PROT N)
STAND-BY (POR)
COMM_LINE
SDA
SCL
DATA-IN-OUT
DATA-CLOCK
SOUND-ENABLE
RESET-AUDIO
DATA-IN-OUT
SDA
DATA-CLOCK
SCL
RESET
HD100
VSYNC
CVBS-TXT
7001 SAA5801H
OTC
EXTERNAL CODE AND DATA INTERFACE
CLOCK GENERATOR AND DISPLAY TIMING
DISPLAY INTERFACE
EPG CLOSE CAPTION TXT
TXT USA
M24C32 7011 NVM
BC847BW
BC857BW
BAT254
OSCOUT
OSCIN
OSCGND
RESET
HSYNC
VSYNC
FRAME
CVBS0
CVBS0_R
CVBS1
CVBS1_R
IREF_DEC
IREF
REF+
STN|BLACK
FADING
DATA
VIDEOn
ROM_OEn
RAM_OEn
ROM_CSn
PSENn
RASn
CASLn
CASHn
WEn
EAn
ROM_OE
RAM_OE
ROM_CS
RAM_CS
RAS
CASL
CASH
WE
+3V3_INTOTC
+5V
+8V
+5V2



	1001 G4	3072 A3
	2001 G3	3073 F3
	2002 G3	3074 F3
	2003 J4	3075 C1
	2004 J4	3076 D4
A	2005 J3	3077 C2
	2006 J3	3078 C4
	2007 J2	3079 A4
	2008 H3	3080 B2
	2009 I8	3081 B3
	2010 I9	3083 D3
	2011 I9	3084 C2
	2012 I9	3085 C4
	2013 G11	3086 D3
B	2014 G11	3087 C3
	2015 G13	3088 C4
	2016 G13	3090 B3
	2017 H12	3091 B4
	2019 E10	3092 D4
	2020 D1	4002 D8
	2022 E2	4003 F1
	2023 A4	4004 F1
	2024 A4	4005 B3
	2025 A5	4006 E4
C	2026 A5	6001 E2
	2027 A6	6003 E3
	2028 A6	7001 A4
	2029 A6	7002 G11
	2031 A9	7003 H12
	2032 E9	7004 H13
	2033 H7	7005 F12
	2034 H8	7006 A9
	2035 H8	7007 F9
D	2036 H8	7008 E1
	2037 H8	7009 D3
	2038 E9	7010 B3
	3001 F3	7011 G2
	3002 F3	
	3003 J3	
	3006 J5	
	3007-A J5	
	3007-B J6	
E	3007-C J6	
	3007-D J6	
	3008-A I6	
	3008-B I6	
	3008-C I7	
	3008-D I7	
	3009 J7	
	3010 I7	
	3011 I7	
	3012 I8	
F	3013 G12	
	3014 G12	
	3015 H12	
	3016 H12	
	3017 G13	
	3018 A3	
	3019 A3	
	3020 A3	
	3021 A3	
G	3023 I8	
	3024 D2	
	3025 E1	
	3026 E3	
	3027 E2	
	3028 I8	
	3029 D8	
	3030 E8	
	3031 D8	
	3032 I8	
H	3033 B4	
	3034 G6	
	3035-A H6	
	3035-B H7	
	3035-C H6	
	3035-D H7	
	3039 B3	
	3040 I2	
	3041 H1	
I	3044-A E2	
	3044-B E3	
	3044-C E3	
	3044-D E3	
	3058 C1	
	3059 B1	
	3060 C2	
	3061 E8	
	3062 A10	
J	3064-A F3	
	3064-B E4	
	3064-C E3	
	3064-D E4	
	3071 A2	

Audio demodulator





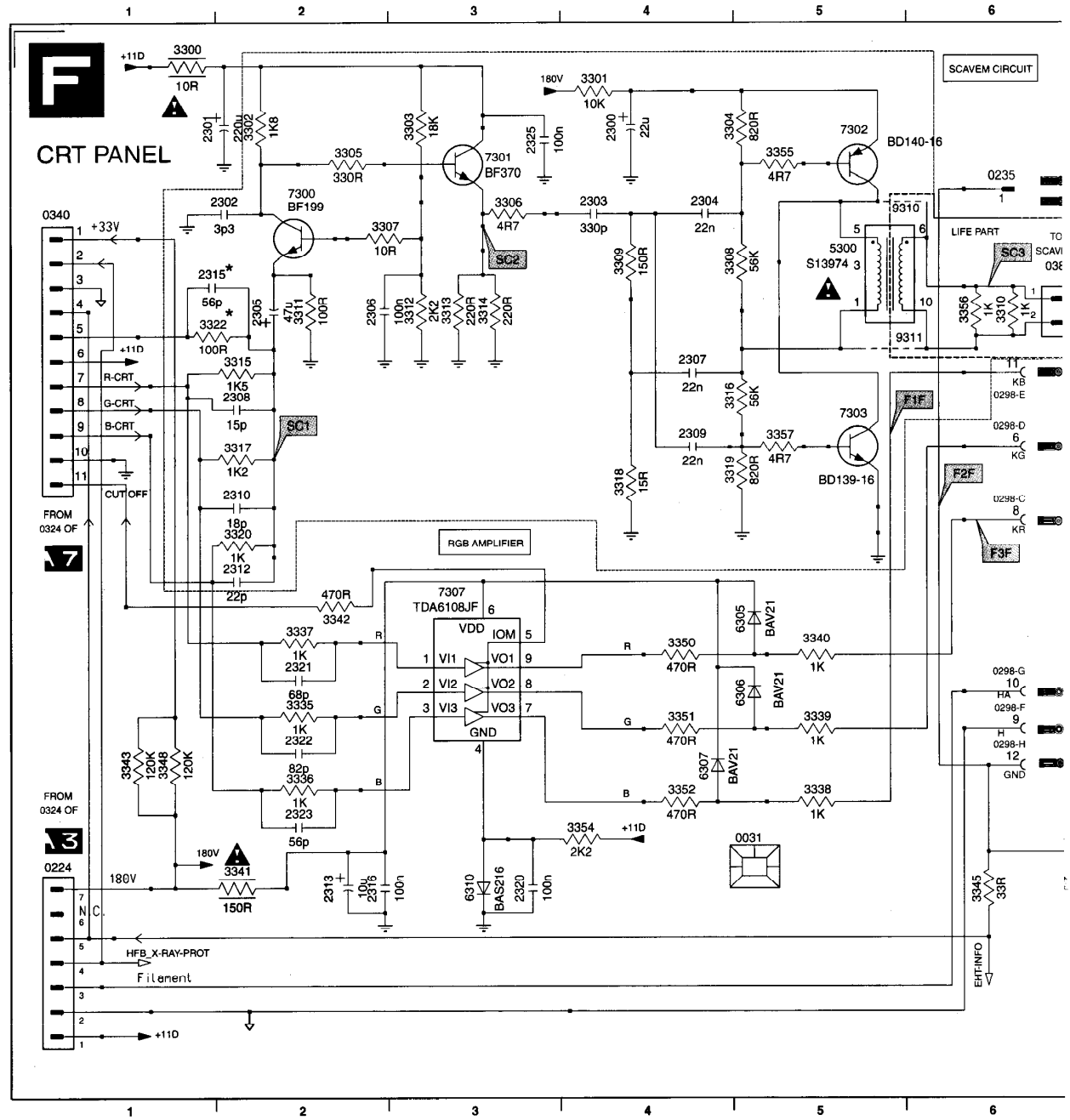
0680 B1	3645 J13	7681 F3
0681 D1	3650 J9	
0682 I7	3651 I1	
1651 H9	3652 H1	
2501 E5	3653 G1	
2502 G2	3654 I1	
2503 F2	3655 B2	
2504 J2	3656 B2	
2505 H2	3657 C13	
2506 E2	3658 C12	
2507 E2	3659 D13	
2508 C9	3660 A12	
2546 G13	3661 C13	
2547 G13	3662 D12	
2548 H14	3663 E13	
2549 J14	3665 F2	
2550 C3	3673 G12	
2551 D2	3676 I14	
2609 C9	3677 H13	
2610 J10	3678 J13	
2611 J10	3679 I13	
2629 A11	3680 B12	
2632 B5	3683 G14	
2634 B6	3684 G1	
2636 C13	3685 F1	
2637 D11	3686 G1	
2638 D13	3687 F1	
2639 B9	3688 J1	
2640 B9	3689 H1	
2641 H13	3690 J1	
2642 J13	3691 H1	
2651 C3	3692 E1	
2652 E5	3693 E1	
2653 D3	3694 E1	
2654 D3	3695 F1	
2655 H4	3696 E10	
2656 H4	3697 F10	
2657 H5	4604 J9	
2658 H5	4605 J3	
2659 E2	4606 H3	
2660 F2	4607 I6	
2661 I2	4608 I6	
2662 G2	4609 I6	
2663 I2	4610 A12	
2664 H2	4612 B5	
2665 J9	4613 B13	
2666 J10	4614 C12	
2667 H9	4615 F13	
2668 H9	4620 I14	
2669 D14	4621 J13	
2670 A12	4630 H8	
2673 B11	4631 H8	
2674 D11	4632 F10	
2675 C14	4633 G10	
2677 C9	4634 H3	
2678 C9	4635 H3	
2679 E11	4650 I13	
2680 E11	4651 J13	
2681 D5	4652 D1	
2682 D5	4653 G14	
2685 F11	4654 F2	
2686 F11	4676 J12	
2690 A9	4677 J12	
2691 B9	4678 F12	
2692 G3	4679 F12	
2693 I9	4680 F13	
3532 A9	4681 F14	
3533 A8	4682 I7	
3540 A9	4683 I7	
3544 B12	4684 I7	
3545 D12	4685 J7	
3546 C13	4686 J7	
3547 E13	4687 J7	
3550 C3	5651 J9	
3551 D2	5652 J9	
3552 F3	5653 C9	
3610 C14	5654 I9	
3611 E14	6651 D3	
3612 G13	6652 C9	
3613 G13	6653 C9	
3614 I14	6654 A9	
3615 J14	7651 D6	
3616 H14	7652-A G12	
3617 F2	7652-B I12	
3621 A12	7656-A B12	
3624 B5	7656-B D12	
3625 B5	7658-A I13	
3630 B5	7658-B J13	
3634 C5	7661 B5	
3636 C13	7663-A C13	
3637 C12	7663-B D13	
3638 D13	7674 B9	
3642 H13	7675-A G4	
3643 I13	7675-B H4	
3644 I13	7680 G13	

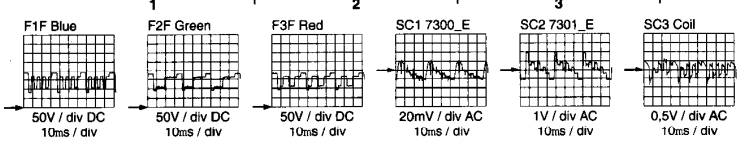
Diversity Small Signal Panel (B6)

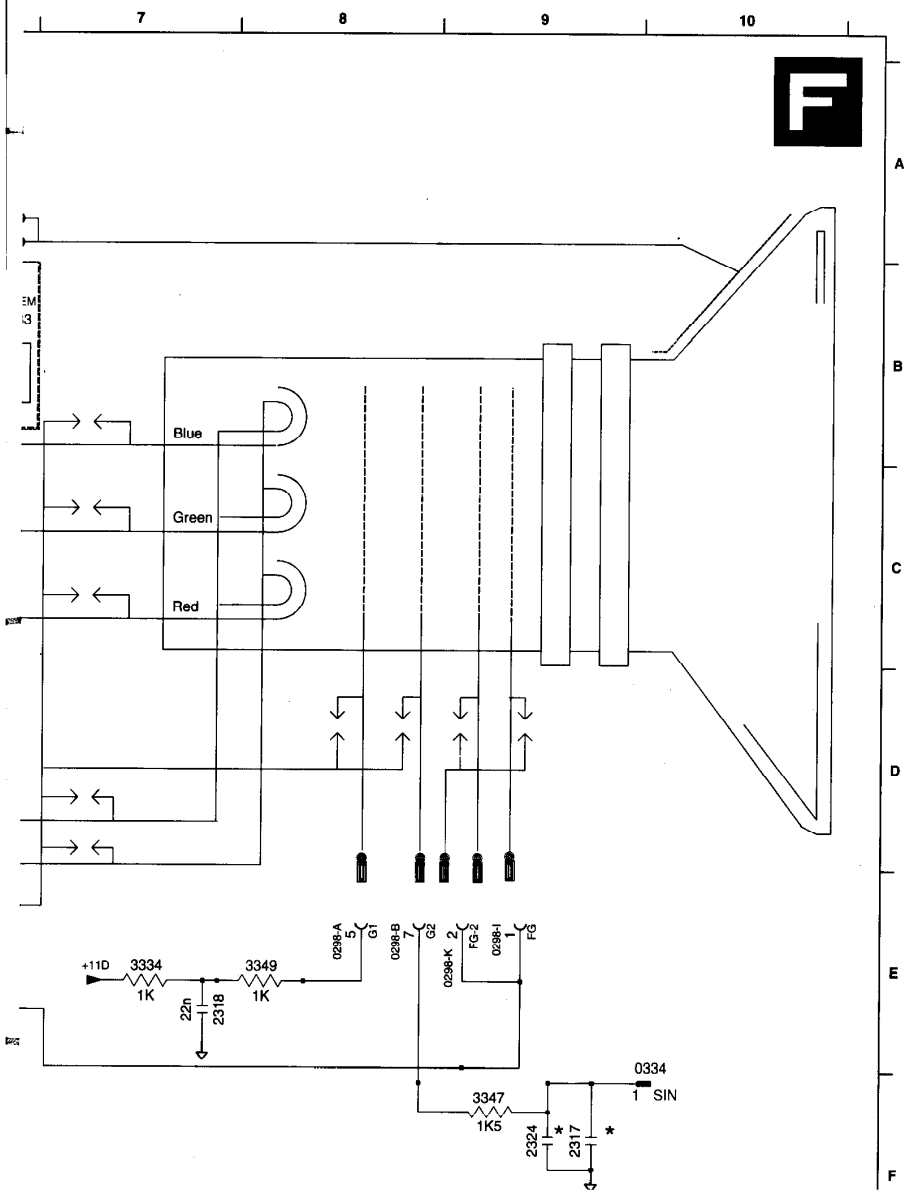
Item	100HZ INCR ST	DS VIRT DLB	100HZ DLB
2636	220N	-	-
2638	220N	-	-
2641	220N	-	-
2642	220N	-	-
2663	-	470P	470P
2664	-	470P	470P
2677	2U2	10U	10U
2678	-	10U	10U
2678	-	10U	10U
2685	-	1N	1N
2686	-	1N	1N
2692	100N	-	-
3532	4K7	-	-
3617	6K8	-	-
3636	1M	-	-
3638	1M	-	-
3642	1M	-	-
3644	1M	-	-
3657	330K	-	-
3659	330K	-	-
3661	1K2	-	-
3663	1K2	-	-
3665	2K7	-	-
3676	1K2	-	-
3677	330K	-	-
3678	1K2	-	-
3679	330K	-	-
4605	-	JUMP	JUMP
4606	-	JUMP	JUMP
4613	-	JUMP	JUMP
4615	-	JUMP	JUMP
4620	-	JUMP	JUMP
4621	-	JUMP	JUMP
4630	JUMP	-	-
4631	JUMP	-	-
4632	-	JUMP	JUMP
4633	-	JUMP	JUMP
4634	-	JUMP	JUMP
4635	-	JUMP	JUMP
4650	-	JUMP	JUMP
4651	-	JUMP	JUMP
4678	-	JUMP	JUMP
4679	-	JUMP	JUMP
4680	JUMP	-	-
4681	JUMP	-	-
7651	MSP3451D-PH-B3	MSP3451G-PH-A1	MSP3451G-PH-A1
7658	BC847BS	-	-
7663	BC847BS	-	-
7675	74HC4052PW	-	-
7681	BC847BW	-	-

CRT panel

0031 E5	0298-G D6	2302 A2	2312 D2	2323 E2	3306 A3	3315 B2	3336 E2	3347 F9	3357 C5	7303 C5
0224 E1	0298-H E6	2303 A4	2313 E2	2324 F9	3307 B2	3316 C5	3337 D2	3348 E1	5300 B5	7307 D3
0235 A6	0298-I E9	2304 A4	2315 B1	2325 A3	3308 B5	3317 C2	3338 E5	3349 E8	6305 D5	9310 A5
0298-A E8	0298-K E9	2305 B2	2316 E2	3300 A1	3309 B4	3318 C4	3339 D5	3350 D4	6306 D5	9311 B6
0298-B E8	0334 F10	2306 B2	2317 F9	3301 A4	3310 B6	3319 C5	3340 D5	3351 D4	6307 E4	
0298-C C6	0340 B1	2307 B4	2318 E7	3302 A2	3311 B2	3320 C2	3341 E2	3352 E4	6310 E3	
0298-D C6	0383 B6	2308 C2	2320 E3	3303 A3	3312 B3	3322 B1	3342 D2	3354 E4	7300 A2	
0298-E C6	2300 A4	2309 C4	2321 D2	3304 A5	3313 B3	3334 E7	3343 E1	3355 A5	7301 A3	
0298-F D6	2301 A1	2310 C2	2322 E2	3305 A2	3314 B3	3335 D2	3345 E6	3356 B6	7302 A5	

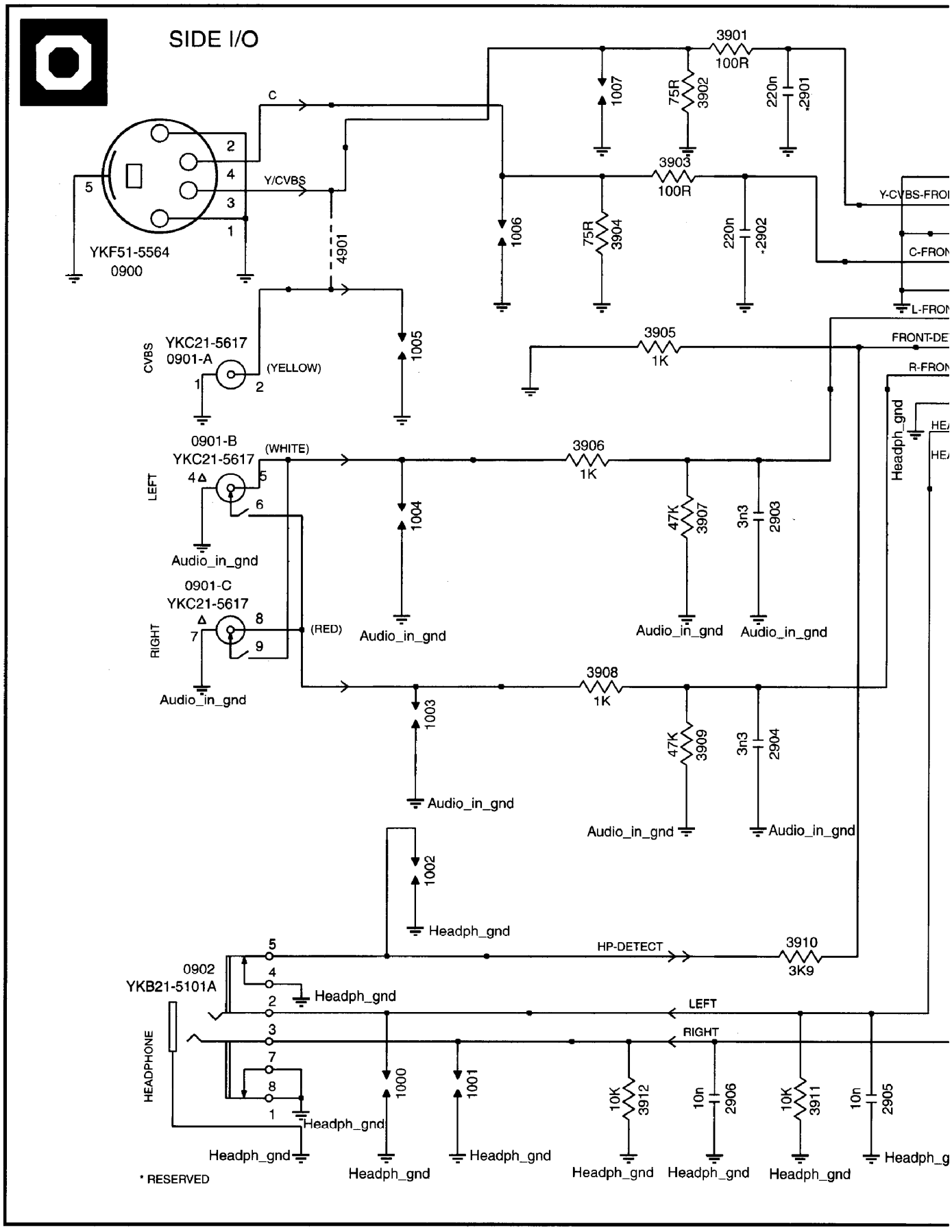


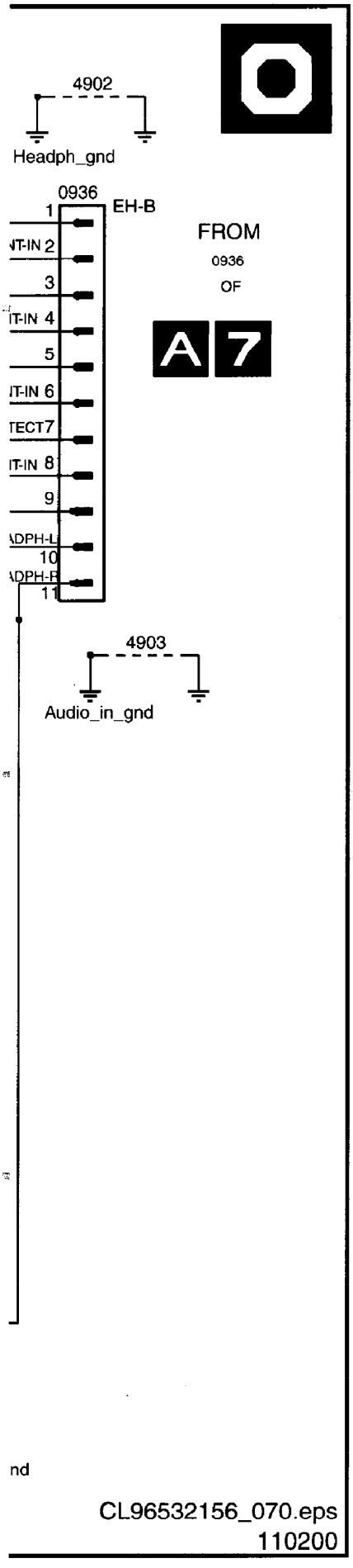




Diversity CRT-Panel					
PosNr	29"	25"	28"	29" WS	32" WS
0298	-	-	-		SOC 9P
0298	CON 8P	CON 8P	CON 8P	CON 8P	-
0383	CON 02P	-	-	CON 02P	CON 02P
2300	22U	-	-	22U	22U
2301	220U	-	-	220U	220U
2302	3P3	-	-	3P3	3P3
2303	470P	-	-	470P	470P
2304	22N	-	-	22N	22N
2305	47U	-	-	47U	47U
2306	100N	-	-	100N	100N
2307	22N	-	-	22N	22N
2308	15P	-	-	15P	15P
2309	22N	-	-	22N	22N
2310	18P	-	-	18P	18P
2312	22P	-	-	22P	22P
2317	4N7	4N7	4N7	4N7	-
2317	4N7	4N7	4N7	4N7	-
2321	-	68P	68P	-	-
2322	-	82P	82P	-	-
2323	-	56P	56P	-	-
2324	-	-	-	-	820P
2325	100N	-	-	100N	100N
3300	FUSE 10R	-	-	FUSE 10R	FUSE 10R
3301	3W 10K	-	-	3W 10K	3W 10K
3302	1K8	-	-	1K8	1K8
3303	18K	-	-	18K	18K
3304	820R	-	-	820R	820R
3305	330R	-	-	330R	330R
3306	4R7	-	-	4R7	4R7
3307	10R	-	-	10R	10R
3308	56K	-	-	56K	56K
3309	150R	-	-	150R	150R
3310	1K	-	-	1K	1K
3311	100R	-	-	100R	100R
3312	2K2	-	-	2K2	2K2
3313	220R	-	-	220R	220R
3314	220R	-	-	220R	220R
3315	1K5	-	-	1K5	1K5
3316	56K	-	-	56K	56K
3317	1K2	-	-	1K2	1K2
3318	15R	-	-	15R	15R
3319	820R	-	-	820R	820R
3320	1K	-	-	1K	1K
3335	100R	-	-	100R	100R
3335	-	1K	1K	-	-
3336	100R	-	-	100R	100R
3336	-	1K	1K	-	-
3337	100R	-	-	100R	100R
3337	-	1K	1K	-	-
3355	4R7	-	-	4R7	4R7
3356	1K	-	-	1K	1K
3357	4R7	-	-	4R7	4R7
5300	TFM	-	-	TFM	TFM
7300	SIGF199	-	-	SIGF199	SIGF199
7301	SIGF370	-	-	SIGF370	SIGF370
7302	TRA POW	-	-	TRA POW	TRA POW
7303	TRA POW	-	-	TRA POW	TRA POW
9305	WR	-	-	WR	WR
9308	WR	-	-	WR	WR
9309	WR	-	-	WR	WR
9312	WR	-	-	WR	WR
9313	WR	-	-	WR	WR
9424	-	-	-	-	WR

Side I/O


SIDE I/O
3901
100R
1007
75R
3902
220n
2901
C
Y/CVBS
3903
100R
1006
75R
3904
220n
2902
4901
YKF51-5564
0900
1005
YKC21-5617
0901-A
CVBS
(YELLOW)
3905
1K
FRONT-DE
R-FRON
Headph_gnd
0901-B
YKC21-5617
(WHITE)
3906
1K
LEFT
1004
47K
3907
3n3
2903
Audio_in_gnd
0901-C
YKC21-5617
(RED)
RIGHT
3908
1K
1003
47K
3909
3n3
2904
1002
Headph_gnd
HP-DETECT
3910
3K9
0902
YKB21-5101A
HEADPHONE
LEFT
RIGHT
1000
1001
10K
3912
10n
2906
10K
3911
10n
2905
* RESERVED


4902
Headph_gnd
0936
EH-B
1
NT-IN 2
3
IT-IN 4
5
IT-IN 6
TECT7
IT-IN 8
9
ADPH-L
10
ADPH-R
11
FROM
0936
OF
A7
4903
Audio_in_gnd
nd
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110200

8.6 Option menu

8.6.1 Introduction:

The microprocessor communicates with a large number of I^2C-IC's in the set. To ensure good communication and make digital diagnosis possible, the microprocessor has to know which IC's have to be addressed. The presence of specific IC's or functions is made known by means of the option codes.

All options codes can be manipulated using both the option numbers and/or the Option menu.
All hardware related options are incorporated under the heading 'Options' of the 'Alignments' sub-menu of the 'Service Alignment Mode'. All software related options that are incorporated under the heading 'Dealer Options' of the 'Service Alignment Mode", can also be reached directly via the 'DEALER' button of the DST.

8.6.2 Options in the Service Alignment Mode

Menu-item	Subjects	Options	Physically in the set
Dual screen/PIP	Aux type	Yes	Dual Screen / PIP module present
		No	Dual Screen / PIP module not present
Teletext/EPG	TXT	Yes	Teletext present
		No	Teletext not present
	NextView present	Yes	NextView set
		No	NextView not set
	NextView type	Flashram	Flash-RAM present
		No Flashram	Flash-RAM present
Communication	Easylink Plus	Yes	Easylink Plus set
		No	Easylink Plus not set
Picture Tube	CRT Type	4:3	4:3 picture tube
		16:9	16:9 picture tube
	Picture Rotation	Yes	Frame rotation circuitry present (diagram A4)
		No	Frame rotation circuitry not present
	Dynamic focus	Yes	Dynamic focus picture tube present
		No	Dynamic focus picture tube not present
	Dooming prevent	Off	
		4:3	
		SF 16:9	
		RF 16:9	
Video repro	Featurebox type	Eco	PROZONIC not present
		Prozonic	PROZONIC present
	Field memories	2	
		3	
	Lightsensor	Yes	Lightsensor present
		No	Lightsensor not present
	PALplus	Yes	PALplus module present
		No	PALplus module not present
	Combfilter	Yes	Not valid for Europe
		No	
	Picture improvement	Yes	
		No	
	Picnic	Yes	PICNIC present
		No	PICNIC not present
	Picnic AGC	Yes	In normal operation: Yes
		No	During 'Drive' alignments: No
	Signalling bits	Yes	
		No	
Source Selection	External 3	Yes	3rd EURO connector present
		No	No 3rd EURO connector present
	External 4	Yes	4th EURO connector present
		No	No 4th EURO connector present
Audio Repro	Dolby	None	
		Pro Logic	
	Rear speakers	Corded	Passive surroundbox present
		Virtual	
		Cordless	Active surroundbox present
	Acoustic system	FL7	Applicable for sets with subwoofer
		FL8	Applicable for sets without subwoofer
		FL9 Monitor	Monitor look (only tweeters at both sides)
		FL9 DAS	FL9 with full range speakers at both sides
	MSP type	MSP3411	
		MSP3415	
		MSP3451	
	AVL enable	On	
		Off	
Miscellaneous	Heatsink Present	Yes	Heatsink present on CRT/SCAVEM panel (diagram F)
		No	Heatsink not present on CRT/SCAVEM panel (diagram F)
	Tuner type	UV1316	
		TEDE9	

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8.6.3 Dealer Options in the Service Alignment Mode

- After the option(s) have been changed, they must be stored via the 'STORE' command.
- The new option is only active after the TV is switched off and then back on again using the mains switch (the EAROM is then read out again).

8.6.4 Option number

In case the EAROM has to be replaced, all the options will also require resetting. To be certain that the factory settings are reproduced exactly, both option numbers have to be set. These numbers can be found on a sticker on the picture tube.

Example: Option number 28PT7306/12 could be:
04929 04418 04417 00016
08199 00001 00000 00000

The first line indicates the hardware options 1 to 4, second line is reserved for the software options.
Every 5-digit number represents 16 bits (so maximum number can be 65536 if all options are set).

Bit	HW1	HW2	HW3	HW4	SW1	SW2	SW3	SW4
0 (1)	FBX (1)		EXT3	MSP (8)	Auto TV	CTI		
1 (2)	FBX (1)	Dolby PL	EXT4	MSP (8)	Auto Store mode (10)			
2 (4)	FBX (1)	Virtual rear spkrs		China IF	Auto Store mode (10)			
3 (8)	Combfilter	Cordless rear spkrs		Tuner (9)				
4 (16)	PAL-Plus	Dolby Digital	Dual Screen (6)	TXT	Picture mute			SLDP (13)
5 (32)	Field mem. (2)		Dual Screen (6)	China TXT	Demo			SLDP (13)
6 (64)	Light sensor	Cabinet (4)	TXT-EPG-DS		Virgin			AVL
7 (128)	LTP	Cabinet (4)	Aux-headphone					
8 (256)	PICNIC	P50	Aspect Ratio (7)					
9 (512)	PICNIC-AGC		Tilt					
10 (1024)			DAF					
11 (2048)	LNA (3)							
12 (4096)	WSS	EPG	Heatsink		TXT pref. (11)			
13 (8192)	Time constant	EPG type (5)	Home Cinema		TXT region (12)			
14 (16384)								
15 (32768)								

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All bits can be set 'On' (= 1) when the option is available or 'Off' (= 0) when it is not, except for:
(1) 0 = Eco, 1 = PROZONIC, 4 = Eco-DNR.
(2) 0 = 2 Field memories, 32 = 3 Field memories.
(3) 0 = Normal, 8192 = Fast.
(4) 0 = FL7, 64 = FL8, 128 = FL9.
(5) 0 = Type 2, 8192 = Type 2C3.
(6) 0 = None, 16 = PIP, 32 = Dual Screen.
(7) 0 = 4:3, 256 = 16:9.
(8) 0 = MSP3415, 1 = MSP3451, 2 = MSP3411.
(9) 0 = Philips, 8 = Alps.
(10) 0 = None, 2 = PDC/VPS, 4 = TXT-Page, 6 = PDC/VPS/TXT-Page.
(11) 0 = TOP, 4096 = FLOF.
(12) 0 = East, 8192 = West.
(13) 0 = Off, 16 = 4:3, 32 = SF16:9, 48 = RF16:9.
When all the correct options are set, the sum of the decimal value (between brackets in 1st column) of each column will give the option number.

9. Circuit descriptions and abbreviation list

9.1 Circuit descriptions

The following circuits are described:
1. Introduction
2. Block diagrams
3. Power supply
4. Control
5. Tuner & IF
6. Video: High-end Input Processor
7. Video: Feature box
8. Video: High-end Output Processor
9. Synchronisation
10. Horizontal deflection
11. Vertical deflection
12. Audio
13. Teletext / NexTView
14. CRT / SCAVEM / Rotation
15. Software related features

9.1.1 Introduction

The EM2E Europe is a lower specified MG-chassis. EM stands for Eco-MG, 2 for the used processor (1 = Painter, 2 = OTC) and E stands for Europe. This will be, at the moment of launch, the cheapest realised 100 Hz set.

The architecture consist of a conventional large signal panel (LSP) and a small signal board (SSB) module, placed into a so called SIMM-connector (Standard Interface, 80 pins).

The LSP is built up very conventional, with hardly any surface mounted components on the copper side. Difference with the MG-chassis is that the EM2E LSP has a very large 'hot' part, including the deflection coil.

The SSB is a high tech module (2 sides reflow technology, full SMC) with very high component density and complete shielding for EMC-reasons. Despite this, it is designed in such a way, that repair on component level will be possible. To achieve this, attention has been paid to:
- The position of service test lands (Tuner side).
- Accessibility (Tuner side).
- Clearance around surface mounted IC's (for replacing).
- Diagnostics & Fault Finding via ComPair.

Due to the low amount of cabling etc., expectation is that the FCR will be low.

Attention: During the first 4 to 6 months of production, the EM2E set-software will be integrated into a flash-RAM on the SSB. After that period, a mask-ROM will be used. Which IC is used is not of interest for service, but for both solutions it means that Service Workshops must be equipped with dedicated (de)solder equipment for exchanging these IC's.
In case flash-RAM or mask-ROM has to be replaced in the field, dealer will receive always an up-to-date flash-RAM.

Warning: Be aware that half of the LSP-circuitry is 'hot', including the deflection coil.

Protection: The start-up behaviour of the EM2E is different then that of the MG-chassis, meaning that there does not exist a situation as in the MG where we have 'supply ON / deflection circuit OFF'.
This means that isolating failures in the EM2E must be done in a different way. See Chapter 5 of this manual.

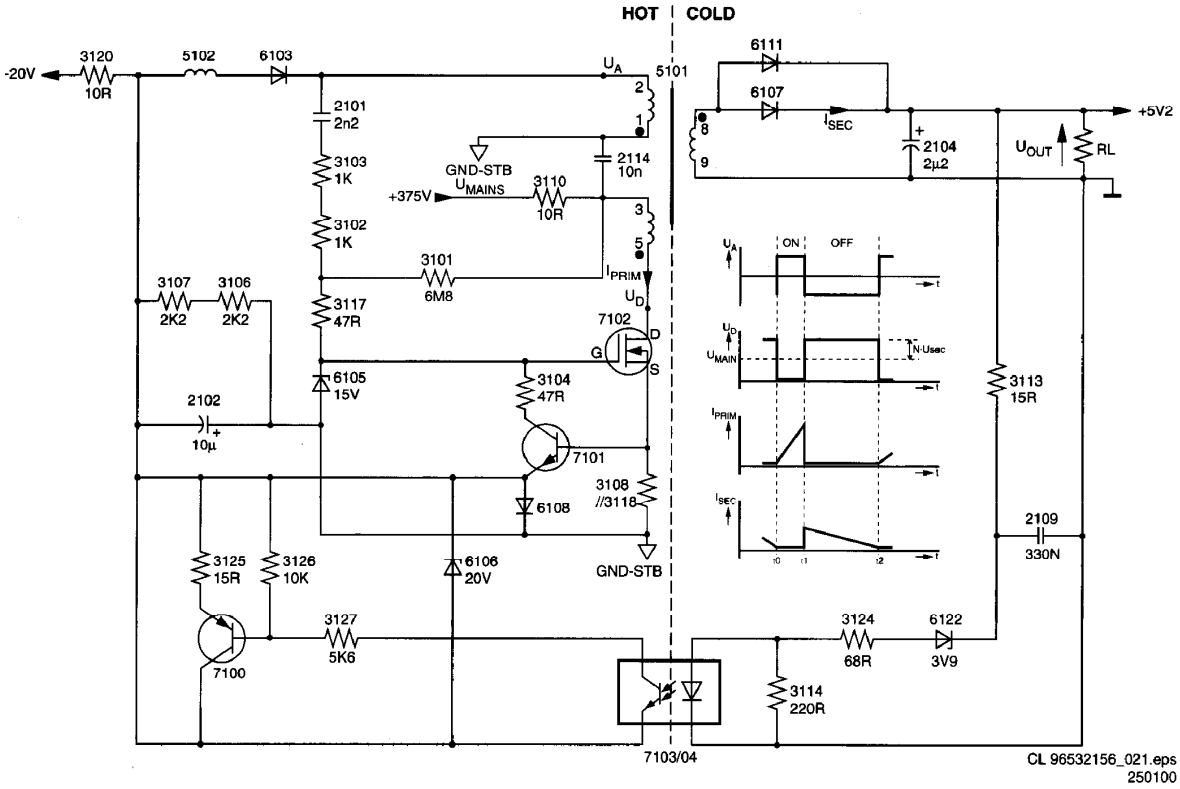

Figure 9-4

To apply this on the EM2E (diagram A2): replace Switch 'S' by FET TS7102, coil L by L5101, diode D by D6107//D6111 and C by C2104.

Time interval t0 - t1:
After switching on the set, the gate of MOSFET TS7102 will be high (max. 15 V due to zenerdiode D6105). This will drive the FET into saturation (U_{DS} = 0 V). The DC-voltage U_{MAINS} will be transposed across the primary winding of L5101 (3, 5) resulting in a linear increasing current through this coil.
The voltage across the co-coupled coil (1, 2) is also positive and will keep the FET into conductivity via C2101, R3103, R3102 and R3117 for some time. The slope of the primary current is determined by the self-induction of the coil and on the magnitude of the supply voltage (+375 V).
The maximum current is determined by the time the FET stays into conductance (t0 - t1). This time is directly determined by the voltage across R3108//R3118. This voltage is a measure of the current and if it exceeds 1.4 V, TS7101 will be driven into conductivity and consequently connect the gate of TS7102 to earth; the FET will block. The current will be: 1.4 V / (15//4.7 ohm) = 0.39 A.
The voltage across the secondary winding (8,9) will be negative, diodes D6111 and D6107 will block.

Time interval t1 - t2:
The sudden current interruption in the primary coil, will induce a counter-e.m.f. that wants to maintain the current. The voltage on the drain of the FET will increase. The secondary voltage (8, 9) will become positive and will charge C2104 via D6107 and D6111. All energy that was stored in L5101 during t0 - t1 will be transferred into the load. Due to the transformer principle, a voltage will now be induced in the primary winding (3, 5) and the co-coupled winding (1, 2). This voltage will be: N * U_{SEC} (N = winding ratio).

The voltage across the co-coupled coil will be negative, keeping the FET blocked.

Time t2:
At t2, the current through the secondary coil will be reduced to zero, as C2104 is no longer charged. As a consequence, the voltages will decay and will change polarity. The gate of the FET will be again made positive, is driven into conductivity and the cycle starts again.

Feedback, stabilisation:
The Standby Power Supply always oscillates at maximum power, the only limiting factor is the maximum primary current which has been pre-set with R3108//3118.
U_{OUT} is determined by R3114, R3124 and zenerdiode D6122. If the voltage across R3114 exceeds the threshold voltage of the diode of the optocoupler 7104 (±1 V) or, in other words, U_{OUT} exceeds 5.2 V, the transistor of the optocoupler will conduct.
Transistor TS7100 will be driven and a negative voltage will be transposed to the emitter of TS7101. When TS7101 conducts, the gate of the FET is at earth potential forcing the oscillator stop. Due to the load, the secondary voltage U_{OUT} will decrease. At a certain voltage, optocoupler TS7103/04 will block and the oscillator will start again.
Since there are no capacitors and there is a high amplification-factor in the feedback circuit, the feedback is ultra-fast. This is why the ripple on U_{OUT} is minimal. The negative supply voltage (-20 V) used in the feedback circuit originates from the co-coupling coil and is rectified through D6103.
Stabilisation is not effected through duty-cycle control but through burst-mode of TS7100.
Burst-mode is load dependent. If the power supply is less loaded, the secondary voltage will have the tendency to increase more rapidly. If the load on the power supply

increases, then the oscillator stops less often, right up to the moment that the oscillator is operating continuously: maximum load. If the power supply is now loaded even more, the output voltage will decay. The maximum load is determined by the maximum primary current set by R3108//3118.

Protection:
If the optocoupler would fail, the secondary voltage will increase. This would have disastrous consequences since many IC's (e.g. OTC, flash-RAM, DRAM) are fed with this 5.2 V. In other words, very expensive repairs would be required. We already know that the negative supply is directly dependent upon the secondary 5.2 V, as a consequence of which the negative supply will increase proportionally as the secondary voltage increases.
If the negative supply in the mean time reaches -30 V, D6106 will start to zener and as a consequence TS7101 will start conducting. Basically, D6106 will take over the stabilisation task of the optocoupler, however, with a considerable spread: from -20 V to -30 V is a 50 % increase, thus U_{OUT} will increase from 5.2 V to max. 7.5 V.

Main supply (diagram A1)

Some important notes on beforehand:
- V_{BAT} is not isolated from the mains supply ('hot').
- V_{BAT} is alignment free.

The Main Power Supply, generates the 141 V (V_{BAT}) and the 28 V for the audio part and is based on the so-called 'down converter' principle.

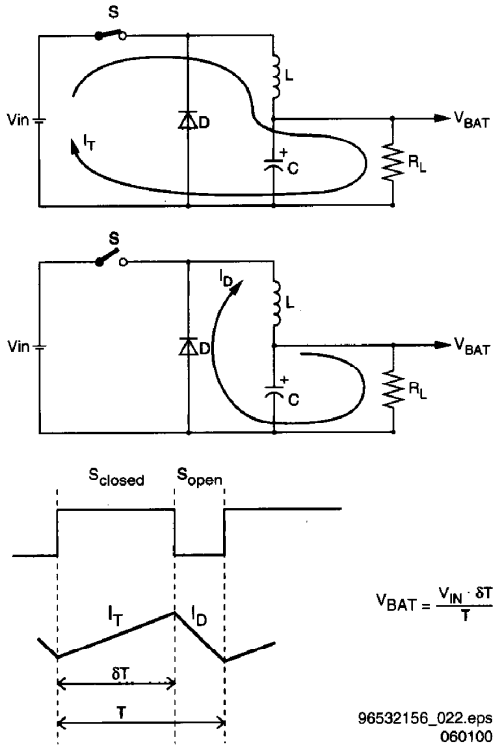

Figure 9-5

- After closing switch 'S', the linear in time increasing current I_T, , will charge capacitor C.
- Opening switch 'S' will generate a counter-e.m.f. in coil L, trying to maintain current I_T. This is possible via diode D (this diode is also called 'freewheel diode'). So after opening 'S', the magnetic energy stored in coil L will be transferred to electrostatic energy in capacitor C. The V_{IN} will only supply current during the time that 'S' is closed while a constant current is flowing through R_L.
- V_{BAT} is directly proportional with V_{IN} and the time that 'S' is closed and reverse proportional with period time 'T'. So by changing the duty cycle, it will be possible to control V_{BAT}.

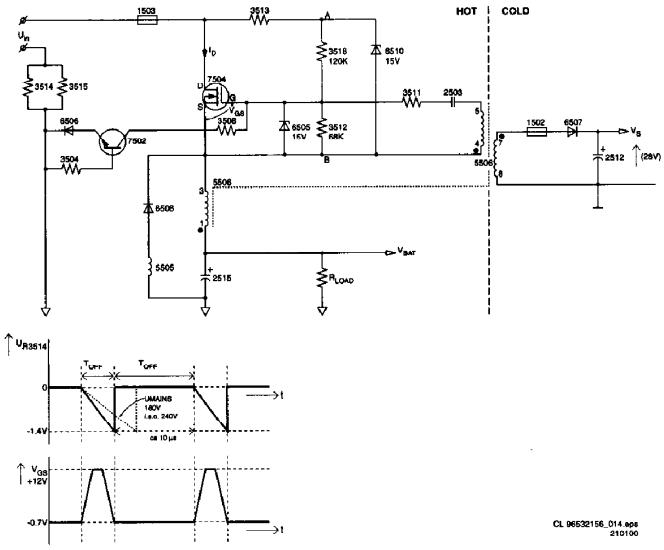

Figure 9-6

At start-up of the main supply, C2515 can be assumed as being a shortcircuit. U_{AB} will be 15 V (R3513, D6510) and U_{GS} of the FET will be +5.4 V (voltage division over R3512 and R3518). The FET will be driven into saturation (same as closing switch 'S'). The drain-current will increase linear in time. With other words: resistors R3513 and R3518 will start the oscillator. The voltage across the co-coupled coil (4, 5) is also positive and will keep the FET into conductivity.

The drain-current will also flow through R3514//R3515. The voltage on the base of TS7502 will be +0.8 V due to the stabilisation circuit (which is explained further). At increasing current, the emitter-voltage of TS7502 will get more negative. When this voltage reaches -0.7 V, TS7502 will be driven into conductivity and consequently connect the gate of TS7504 to earth; the FET will block (same as opening switch 'S'). The maximum drain-current is: 0.7 V / (R3514//R3515) = 1.4 A. The voltage polarities on L5506 will invert, keeping the gate of TS7504 negative via the co-coupled coil (4, 5). The voltage on the secondary winding of L5506 (7, 8) will be positive, generating the +28 V audio supply voltage via D6507 and C2512.

The sudden current interruption in the primary coil, will induce a counter-e.m.f. that wants to maintain the current via the 'freewheel' diode D6508. This current is linear decreasing in time and as it is also flowing through R3414//R3415, TS7502 will be blocked after a certain time period. The gate of the FET will be again made positive, is driven into conductivity and the cycle starts again.

Stabilisation of V_{BAT}:
The output voltage V_{BAT} will be determined by: $V_{BAT} = V_{IN} * T_{ON} / (T_{ON} + T_{OFF}) = V_{IN} *$ duty-cycle.
To stabilise the output voltage, a feedback loop is implemented, which will reduce T_{ON} when V_{BAT} increases and vice versa.

Via a voltage divider, excisting of (1 %) resistors R3507, R3510 and R3527, a voltage of 2.5 V (when V_{BAT} = 141 V) is fed to the input of precision shunt regulator 7506. This regulator will

conduct, a current will flow through R3524 and TS7505 will be driven into conductivity. The base of TS7502 will now be set at a certain positive voltage. As this transistor switches the FET TS7504 on and off, this circuit can determine the dutycycle.

E.g. when the load increases, V_{BAT} will decrease. As a consequence, the input-voltage of regulator 7506 will decrease, resulting in a lower current. Through that the emitter-base voltage of TS7505 will diminish.
The current through R3504 will decline, changing the base-voltage of TS7502 and through that the T_{ON} (will increase) of the FET. The output voltage V_{BAT} will rise.
If the load continues to increase, the regulator will block at a certain moment, the collector-current of TS7505 will now be zero. If there flows no current through R3504, T_{ON} will now be maximum (I_{MAX} = 1.4 A). This is the point where V_{BAT} will be below 141 V, and at further increasing load will be switched off (The voltage across the co-coupled coil (4, 5) will decrease due to the increasing load. Therefore the voltage on the gate of TS7504 comes below the threshold voltage. The supply switches off and an audible hiccuping can be heard).

On the other hand when the load decreases, V_{BAT} will rise. As a consequence, the input-voltage of 7506 will also rise resulting in a higher current. The current through R3504 will rise, changing the base-voltage of TS7502 and through that the T_{ON} (will decrease) of the FET. The output voltage V_{BAT} will be reduced.

If, for instance, V_{IN} will decrease (e.g. U_{MAINS} is 180 V i.s.o. 240 V), the slope of the drain-current will be flattened, through which the FET will be longer into conductance, keeping V_{OUT} constant.

If, for any reason, the stabilisation circuit might fail, the output voltage V_{BAT} can never exceed 200 V (via D6514). D6514 will form a shortcircuit, V_{BAT} will drop and the set will switch off (this will result in an audible hiccuping of the supply).

Set to 'STANDBY" (via RC):
When the set is switched to 'STANDBY' via the Remote Control, the Main supply will be switched off.
This is done by the circuit around TS7529 (see diagram A1):
During 'ON'-state the Main supply is fed with line pulses via the STANDBY line. They are rectified and smoothed via D6517, D6516 and C2530 and fed to TS7529. Because they are less than -20 V, this transistor will be blocked.
When these pulses are stopped (STANDBY), TS7529 will be saturated and TS7502 will be switched off. This will switch off the Main supply.

Set to 'ON' (via 'STANDBY'):
At the moment the set is switched 'ON', the HOP is not working (as much as possible IC's are made voltageless during 'STANDBY'). Therefore it is impossible that the STANDBY line carries line-pulses, so the main supply cannot start up. This problem is solved via the 'low power start-up' possibility of the HOP.
Via pin 22, the HOP receives, via the STANDBY_INFO line from the OTC, a voltage of 5.2 V coming from the Standby supply. The result will be that the HOP will generate pulses with a nominal T_{OFF} and T_{ON} growing from 0 to 30 % of the nominal value.
This signal is unchanged until the Main supply is switched 'ON' and the HOP the correct I^2C-command POR-bit) has received.

Guarding circuit:
The negative pulses on the secondary winding of L5506 are rectified by D6520 and smoothed by C2535. The resulting negative DC-voltage will keep TS7510 blocked, even as TS7511.

When something happens in the Main supply through which these pulses will decrease, the DC-voltage will increase. TS7510 starts to conduct, even as TS7511. Via R3541 and D6522 this situation will be maintained (thyristor principle). The collector of TS7511 drives via R3538 a positive pulse back to the OTC (named STANDBY(POR)). The OTC will now switch off the Main supply via the STANDBY_INFO signal.

SSB

There are 5 different voltages located on the SSB: +33 V, +11D V, +8 V, +5.2 V and +5 V.
+5.2 V is the Standby voltage, it should always be present. The 8 V is derived from the 11D V with stabiliser 7906. The 11D voltage is only present when the line-drive pulses start the deflection.
The 8 V is used to switch the +5.2 V with transistor 7905 to supply the +5 V.

9.1.4 Control (diagram B5)

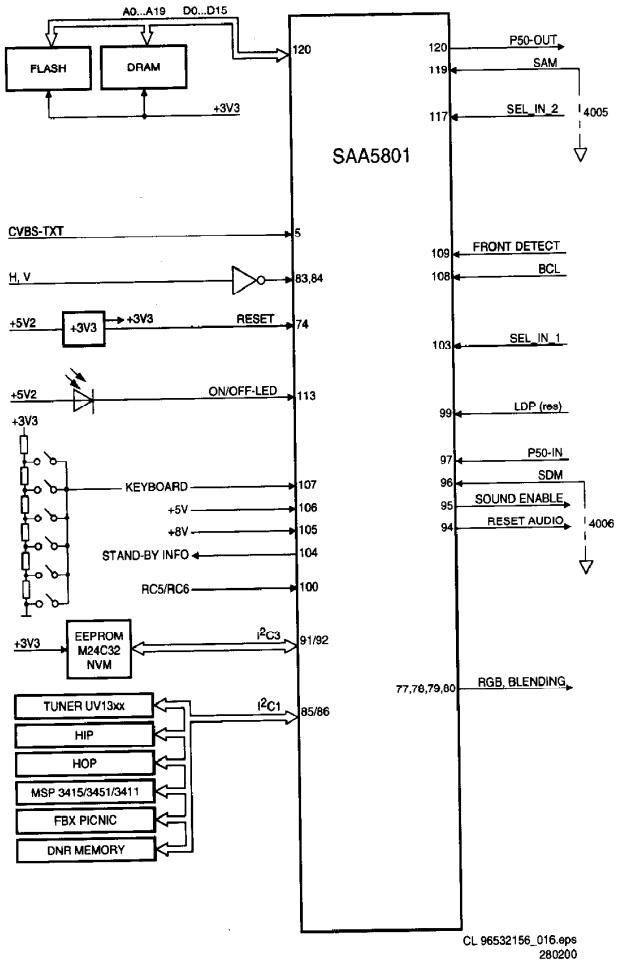

Figure 9-7

OTC

The SAA5801 (IC7001) is called the OTC (OSD, TXT and Control). In this IC, the microprocessor and the TXT-decoder (level 2.5) are integrated.
Some of its functions are:

- Set control.
- TXT/OSD acquisition.
- RGB-outputs to the HOP
- Menu blending; for blending the contrast is software controlled.
- I/O-ports for I^2C, RC5, LED, and service modes.
- Error code generation.

The software for EM2E can be 2 MB (Megabyte).
For TXT-data 1000 pages can be stored in IC7007. This is a DRAM of 4 Mbit and this IC is also used to store data of a working set.
The Non Volatile Memory IC7011 is a 4 kB version M24C32W6.

All ICs in this part are supplied with 3V3. For this voltage a 3V3 stabiliser is used (IC7005).
When the 3.3 V is available, a POR is generated with TS7003/7004 to wake up the OTC. During the reset all I/O pins are high. When a POR is generated the TV-set is in Standby mode.

Via pins 105 and 106 the 8 V and the 5 V are sensed. If one of them is not present, the Main supply is switched off (set in protection and the red LED will blink at 3 Hz). The OTC will generate an error code to indicate what was wrong.

The horizontal (HD100) and vertical (VSYNC) sync pulses are also fed to the OTC for stable OSD and TXT.

The RGB-outputs (77/78/79) together with fading (pin 80) are fed to the HOP. The fading pin has a double function: it is used for making a transparent menu and as fast-blanking signal for TXT.

I^2C-busses

In the EM2E-chassis with OTC-processor there are two I^2C-busses used:

- Slow (max. 100 kHz) hardware I^2C-bus (called I^2C1), used for all IC communication.
- Separate short bus (called I^2C3) for the Non Volatile Memory (NVM) to avoid data corruption.

NVM

The Non Volatile Memory contains all set related data that must be kept permanently, such as:

- Software identification.
- Operational hours.
- Error-codes.
- Option codes.
- All factory alignments.
- Last Status items for the customer + a complete factory recall.
- Txt featuring (keeping habit watch data).
- EPG data.

9.1.5 Tuner & IF (diagram A7 & B2)

The tuner UV1316 is I^2C-controlled and is capable of receiving off-air, S- (cable) and Hyperband channels:

- Low 44 - 156 MHz
- Mid 156 - 441 MHz
- High 141 - 865 MHz

The tuning is done via I^2C. The reference voltage on pin 9 is 33 V. This voltage is derived from the 180 V (from the LOT) via a resistor of 120 kΩ and a zenerdiode. The OTC together with the HIP control the tuning procedure. There is also automatic switching for the different video systems.

The IF-filter is integrated in a SAW (Surface Acoustic Wave) filter. The type of this filter is depending of the standard(s) that has to be received. Two SAW filters are used: One for filtering picture-IF and the second-one for sound-IF. An extra filter (5403), tuned at 40.4 MHz, is necessary for L/L' sets with 6.5 MHz sound to suppress the neighbour channel.

The output of the tuner is controlled via an IF-amplifier with AGC-control. This is a voltage feedback from pin 62 of the HIP to pin 1 of the tuner. AGC take-over point is adjusted via the service alignment mode 'Tuner AGC'. If there is too much noise in the picture, then it could be that the AGC setting is wrong. The AGC-setting could also be mis-aligned if the picture deforms with perfect signal. The IF-amplifier amplifies too much.

The video IF-signal is fed to pins 2/3 of the PLL-controlled IF-demodulator. The voltage controlled oscillator of the PLL is adjusted via the service menu 'IF AFC'. If the alignment is correct then the displayed frequency in the installation menu is the same as the applied frequency from a generator. The external coil L5408 connected between pins 7/8 is used as reference. The demodulated IF-video signal is available at pin

10 of the HIP. In this video signal there is a rest of sound carrier, which is filtered by the sound trap 1407.
Then the signal is again fed to the HIP on pin 12 where the group delay can be corrected, dependent on the standard that is received. On pin 13 the CVBS-signal becomes available which is used for further processing in the television. Via TS7322 the signal is supplied to EXT1 and back into the HIP on pin 14 to the source/record selection.

To realise quasi split sound the IF-signal is fed to the HIP on pin 63/64 via SAW-filter 1405. The FM (or AM for L-norm) - modulated signal is available on pin 5 and is fed to the audio demodulator MSP34xx.

9.1.6 Video: High-end Input Processor (HIP, diagram B2))

In the EM2E the TDA932xH input processor is used, which contains the following functions:
- IF demodulation.
- Group delay correction.
- AFC signal generation, used to track drifting transmitters.
- Sound carrier re-generation (SIF).
- AM demodulation.
- Sync acquisition, delivering HA and VA.
- Switching off IF-filtering.

The HIP has various inputs.
- Full matrix switch with:
  - 2 CVBS inputs
  - 2 Y/C (or additional CVBS) inputs
  - 1 CVBS front end input
- Two RGB inputs and 2 status-inputs

Outputs: Three separate switchable outputs can be used:
- 1 YUV-output is fed to the PICNIC
- 2 CVBS outputs: One for Teletext Dual Screen and the other for output to EXT2 to have WYSIWYR (What you see is what you record)

I/O-switching: The external signals are fed directly to the I/O part of the HIP with status from pin 8 of SCART. On the HIP there are two status inputs available (pins 15, 17) with two voltage levels:
- 4:3 -> 2.2 V
- 16:9 -> 5.5 V

The input signals from the Front I/O are fed to the HIP and front detection is also fed to the OTC.
EXT1 is full SCART: thus CVBS and RGB. The RGB-selection is done in the HIP.
EXT2 is meant for VCR and has therefore some additional signals in relation to EXT1 but no RGB. EXT2 has also the possibility for Y/C_in and Easylink-Plus (P50). Y_in is with pin 20 and Chroma in with pin 15. Easylink is handled via pin 10 of the SCART and this is a bi-directional communication.

Easylink supports the next features:
- Signal quality and aspect ratio matching
- One touch play
- One touch text
- PIP
- Pre-set download
- WYSIWYR
- Automatic Standby

With Easylink-Plus is added:
- Country and language installation
- System Standby
- Intelligent set top box features
- NexTView download
- Timer record control
- VCR control feature

Video processing
The sandcastle-pulse of the HIP will not be used for synchronisation. The HOP will generate synchronisation signal derived from the feature box (PICNIC) signals. If a VCR is connected, there is also an automatic correction for Macrovision. This is active for the external sources and the pre-sets 0, 90-99.
The HIP itself (no external voltage) controls the Y/C switch in the HIP.
The chrominance decoder in the HIP is full multistandard: PAL/SECAM/NTSC.
Two different crystals can be connected to the pins 54 & 57 without any alignment. The crystals are also used as a reference for the synchronisation. A digital control circuit that is locked to the reference signal of the colour decoder determines the start-up of the sync. This crystal may only be replaced by the original one. If just a crystal is taken, the internal capacitance will be different and the effect will be that there is no colour.
In the HIP a sync separation has been integrated; the HIP delivers the HA and VA 50Hz/60Hz to the PICNIC. On pin 59 there is the 1fH sandcastle but this is not connected to any circuit and only used internally for the colour demodulator. The 2fH-sandcastle signal is generated by the HOP.

9.1.7 Video: Feature box (PICNIC, diagram B3))

Introduction
The basic function of the Feature box (FBX6) is picture improvement, and depending on the version, several scan conversion methods can be applied. The PICNIC (SAA4978H) is the central key component.
In the EM2E-chassis the featurebox is integrated on the SSB. The PICNIC is used for the 100Hz conversion. In the PICNIC the following functions are present:
- The ADC.
- The DAC.
- The 100 Hz conversion.
- The Panorama mode.
- The noise limiter (DNR).
- The contrast improvement.

All these functions are integrated in one IC: SAA4978H, 160 pins QFP

ADC/DAC
Analogue to Digital conversion is done with three identical 9-bit ADC's.
Digital to Analogue conversion uses three identical 10-bit DAC's.
In the PICNIC there are three 9 bits ADCs present for Y,U,V. For digitising the Y (luminance) 9 bits are used, to realise a more detailed picture. The 9 bits are only internally used. Via dithering the 9 bits are reduced to 8 bits and that data is stored into the memory. The data in the memory is fed back to the PICNIC and via undithering the data is again reproduced 9 bits for processing.
U/V (colour difference signals) is also sampled with 9 bits. These two 9 bit data streams are multiplexed to 4 bits data streams. This reduction can be allowed, as the perception for colours by the human eye is less sensitive as for luminance.

100 Hz conversion
The main task of the PICNIC is the conversion from 50Hz to 100Hz for YUV and HV-sync. In order to remove 'large area flicker' (especially visible in a white picture), the field-rate of the video is doubled by the FBX6. A 50/60 Hz frame frequency is converted to 100/120 Hz. Also the line frequency (16 kHz) is doubled (32 kHz). Basically, when the video input contains fields A, B etc..., the conversion provides an AABB sequence on the display. The actual conversion is done in the first Field Memory by reading it twice at double speed, while writing it once.

PROZONIC

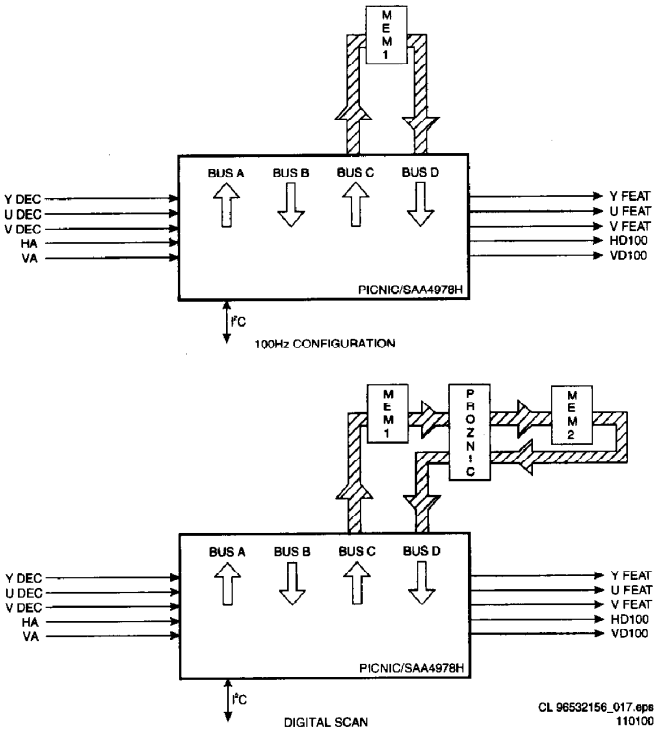

Figure 9-8

To the PICNIC external IC's are connected dependent of the features.
If EM2E has only 100Hz then only one memory-IC is used to store one frame.
For sets with Digital Scan the PROZONIC (IC7708, SAA4990H) has been added with two memory-ICs (IC7714/7715). It is an abbreviation for PROgressive scan Zoom and Noise reduction IC.
When applying this, the 2nd Field Memory has to be installed.
The following functions are available:

- Line flicker reduction (Digital Scan): this is a feature to reduce the 25 Hz interlace line flicker.
- Dynamic Noise Reduction: noise affected signals can be improved by combining the pixel values of the current and past video fields. This is however only possible in areas without movement.
- Variable Vertical Sample Rate Conversion
- Synchronous No Parity Eight bit Reception an Transmission interface (SNERT-bus)

Depending on the chassis model, the FBX6 can have the following specification:

Featurebox 6 diversity	
Set	Chipset
EMG 1fH	
EMG 2fH	1 Memory
EMG 2fH DNR	1 Memory incl. DNR
EMG 2fH Dig. Scan	PROZONIC + 2 Memories

Dual Screen compression
The PICNIC can provide horizontal video compression up to 50 %. The compress mode can be used to display dual screens for instance with Teletext (only for widescreen sets).

Panorama
To fit 4:3 pictures into a 16:9 display, a panoramic horizontal distortion can be applied to make a screen-fitting picture without having black sidebars or lost video.
The centre horizontal gain is programmable and the side gain is automatically adapted to make a screen-fit.

Automatic Aspect Ratio Adaptation (AARA)
This feature uses data from the 'black bar detection circuit' to adapt the vertical and horizontal amplitude to an aspect ratio belonging to the display without showing the black bars.

CTI
At CVBS video signals, the bandwidth of colour signals is limited to 1/4 of the luminance bandwidth. Transients between areas of different colours are therefore not very sharp. The PICNIC can steepen these transients artificially with a time manipulation algorithm.

Dynamic Contrast
To make the contrast (black/white) range wider, Philips has invented Dynamic Contrast. It uses the digital memory used in 100 Hz sets. It measures every A-field (25x/s) and digitally analyses where on the greyscale most of the image is located. If it's a relatively dark image, the lighter part of that image is stretched towards white, so that more contrast will become visible in that picture. If it's a relatively light image, the darker part of that image is stretched towards black, so that these darker parts will have more contrast. When the image is in the middle of the greyscale, both dark and light parts are stretched.

9.1.8 Video: High-end Output Processor (HOP, diagram B4)

General
In the HOP (High-end Output Processor, TDA9330) the video processor and digital deflection processor are integrated. The main functions of the HOP are:

- Video control (contrast, brightness, saturation, etc.).
- 2nd RGB interface for OSD/TXT.
- Peak White Limiting.
- Cut-off control and White Drive (RGB outputs).
- Geometry control.

The YUV-signals from the PICNIC are fed to the HOP. In the HOP, the video and geometry control parts are integrated. Also the RGB-signals from TXT/OSD are inserted via the HOP. This IC has all functions from a video processor and geometry control (like the DDP in MD2). The geometry part delivers the H-drive, EW-drive and also a drive signal for rotation. The internal V-drive circuit of the HOP is not used (is explained further on).

Video Control
After conversion to RGB again, the signals can be controlled for Saturation, Contrast and Brightness.

2nd RGB interface for OSD/TXT
On pins 35 - 38 the RGB and fast blanking from the OTC (OSD and TXT) are inserted.

Peak White Limiting
On pin 43 there is a Peak White Limiting signal line (PWL). If the beam current (EHT-info line) increases, then the EHT-info voltage will decrease. PWL is controlled by average limiting via R3343/C2333.

Cut-off control
Switching the TV to Standby:

1. Vertical scan is completed.
2. Vertical flyback is completed (the horizontal output is gated with the flyback pulse, so that the horizontal output transistor cannot be switched on during the flyback pulse).
3. Slow stop of the horizontal output is started, by gradually reducing the 'on' time at the horizontal output from nominal to zero (this will take 50 ms).

4. At the same time the fixed beam current is forced via the black current loop for 25 ms. This is done by setting the RGB outputs to a maximum voltage of 5.6V.

In the EM2E a 'one-point' cut-off control is used:
A current of 8 µA (for cut-off) is fed to pin 44 of the HOP. This is done with a measurement pulse during the frame flyback. During the 1st frame, 3 pulses are generated to adjust the cut-off voltage at a current of 8 µA.With this measurement the black level at the RGB-outputs is adjusted. So at start-up there is no monitor pulse anymore. At start-up, the HOP measures the pulses which come back via pin 44. The RGB-outputs have to be between 1.5 V and 3.5 V. If one of the outputs is higher than 3.5 V or one of them lower then 1.5 V, the RGB-outputs will be blanked.

Geometry control
All geometry control is done via I^2C and the data is stored in the NVM (IC7011) of the SSB.

Line drive (LINEDRIVE1).
Line drive is derived from an internal VCO of 13.75 MHz. As a reference an external resonator is used (1301). The internal VCO is locked with the HD100-pulse, which comes from the PICNIC. The 'PHI-2' part in the HOP receives the HFB_X-RAY_PROT (pin 13) to correct the phase of the line drive. The EHT-info is supplied to pin 14 (DYN-PHASE-CORR) to compensate picture breathing depending on the beam current. Service tip: This is not used at the moment, therefore EHT-compensation in the service menu is put to zero.

Frame drive (FRAMEDRIVE+).
The VD100 signal from the PICNIC will be extended for 16.5 lines by the circuit around TS7309 and 7311. The resulting signal (VDHOP) will drive TS7310. This will result in the (asymmetric) FRAMEDRIVE+ signal.
Note: The Frame outputs (pins 1/2) of the HOP are not used!

East/West drive.
At pin 3 the E/W-drive is available. Pin 4 is a feedback input for the EHT-info and is used to prevent pumping of the picture. EHT varies also dependent of the beam current. For widescreen without load this is 31.5 kV and with load (1.5 mA) 29.5 kV.

Frame rotation (only for 16:9 sets):
For frame rotation a control voltage is used from pin 25 of the HOP. This voltage can vary from 0.4 V till 4 V.

Guarding protections:
- Flash detection:

When a flash occurs, the EHT-info will become negative very fast. Via D6303/D6304/R3316, TS7303 starts to conduct. This makes pin 5 of HOP high. When pin 5 of HOP is high, then the output (pin 8) is immediately stopped. If H-drive stops then also pin 5 will be low again, which will reset the flash detection. A bit (FLS) will be set in an output status register, so via the OTC it can be seen when there was a flash. This FLS-bit will be reset when the OTC has read that register.
- HFB protection:

If the HFB is not present then this detected via the HOP. The OTC puts the TV into protection and reads a register in the HOP. An error code will be generated.

9.1.9 Synchronisation (diagram B3 & B4)

The HIP video processor provides vertical and horizontal sync pulses VA and HA that are synchronised with the incoming CVBS signal. These pulses are fed to the PICNIC where they are doubled to be synchronous with the 100 Hz picture. The outgoing pulses, VD100 and HD100 are fed to the HOP that supplies the vertical and horizontal drive pulses and the 100 Hz (2fH) sandcastle pulse.

The VD100 pulse from the PICNIC is only one line long. Therefore this pulse is converted into a VDHOP signal by a 530 µs monostable oscillator (extended by 16.5 lines). This signal is on block function level equal to VSYNC and FRAMEDRIVE+.

The OTC is synchronised on the HD100 pulse from the FBX and on the VSYNC for the synchronisation of TXT/OSD/EPG

When no CVBS is offered to the video processor, the VA and HA pulses are switched off by the HIP, and the VD and HD pulses are then generated by the PICNIC. This to assure a stable OSD.

9.1.10 Horizontal (line) deflection (diagram A3)

Driving the line output stage

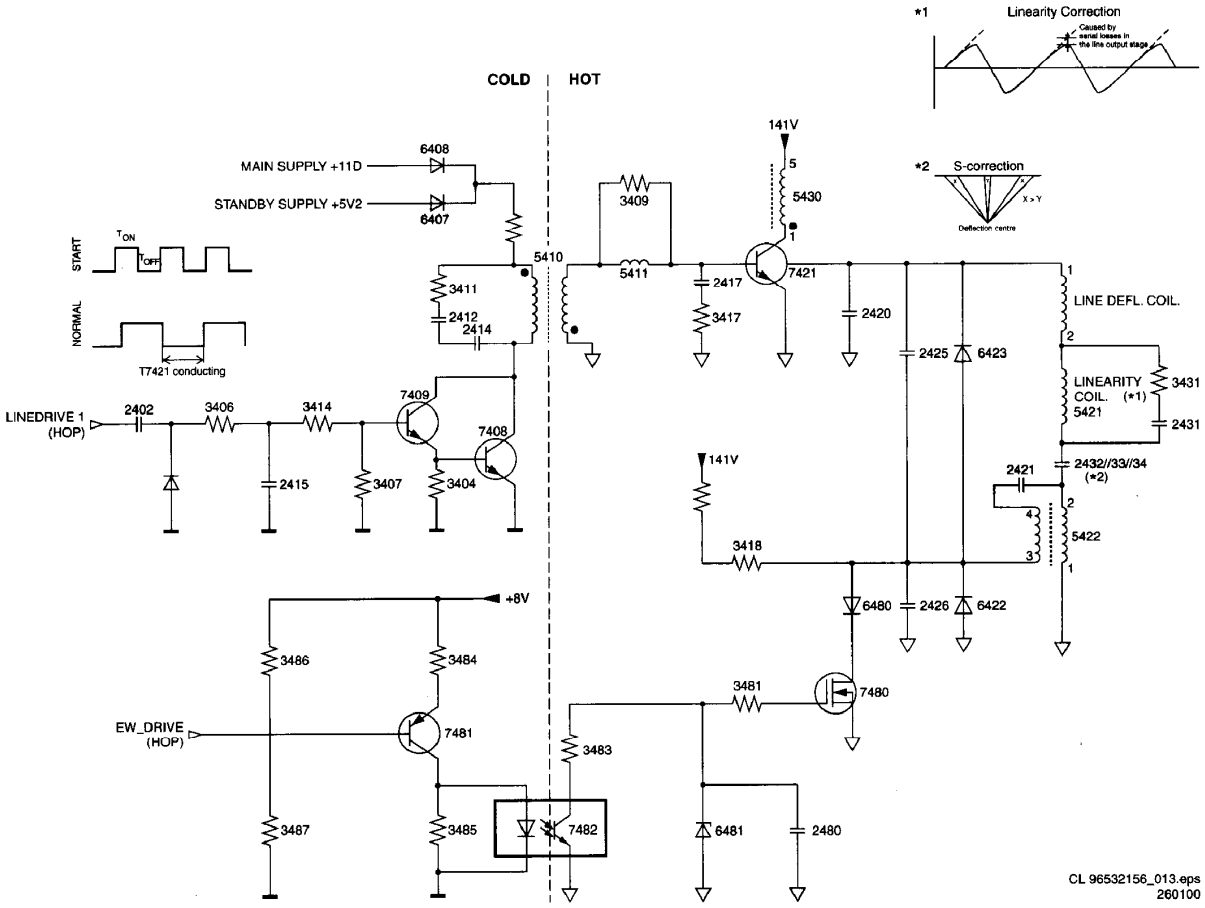

Figure 9-9

The HOP (located on the SSB) generates the line-drive pulses (LINEDRIVE1), which have a frequency of 31250 Hz (T = 32 µs).

When the LINEDRIVE1 signal is high, TS7409 and TS7408 will conduct. A constant DC voltage will be applied across L5410, causing a linear increasing current through this coil. The secondary voltage of L5410 has a negative polarity so that TS7421 will block. When switching on the set, the current through L5410 is supplied by the 5V2 Standby supply (via D6407), and taken over by the +11D voltage (via D6408) of the main supply.

When the LINEDRIVE1 signal becomes low, TS7409 and TS7408 will block. The voltage polarity across the primary winding of L5410 will invert. The positive voltage on the secondary winding will now drive TS7421 into conductivity. Because of the storage time of the line transistor (TS7421), L5410 cannot transfer its energy immediately to the secondary side. This may result in high voltage peaks on the collector of TS7409 and TS7408. To prevent that these peaks will damage the transistors, a 'snubber' circuit (C2414, C2412 and R3411) will suppress them.

When the LINEDRIVE1 signal is high again, the above-described sequence starts again. Circuit L5411 and R3409 will increase the switch-off time of the line transistor.

The line stage will be started via the 'slow start' principle. During start-up, the HOP generates line drive pulses with a small T_{ON} and a high frequency (50 kHz); T_{OFF} will be constant and T_{ON} will be gradually increased until the duty-cycle is 50 % (normal condition). The time interval from start to normal condition takes about 150 ms. When switching off, the same procedure is followed, but now in reverse order.

Operation of the line output stage

To explain the operation of the line output stage, we use the following start conditions:

- C2433 is charged to max. 141 V (V_{BAT})
- TS7421 is driven into conductivity.

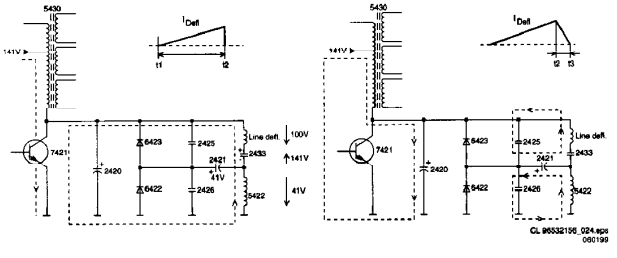

Figure 9-10

Period t1 - t2:
When TS7421 is driven into conductivity, the capacitor voltage of 141 V, will be divided across bridgecoil L5422 and the deflection coil (conn. 0317). Due to the chosen inductance values, there will be 100 V across the deflection coil and 41 V across L5422. The linear increasing current in the deflection coil will result in a spot moving from the centre of the picture tube to the right.
The voltage across L5422 will also charge C2421 (41 V - 0.7 V).

Period t2 - t3:
At the moment the LINEDRIVE signal becomes high, TS7421 will stop conducting. In the coils a voltage will be induced, trying to maintain the current. The current through the line deflection coils continues to flow through C2425 and C2421 and the current through L5422 continues to flow through C2426 and C2421. The energy stored in the line deflection coil is passed to C2425, and the energy of L5422 to C2426.
The resonance-frequencies of these 2 LC-circuits define the flyback time of the spot from the right side of the picture tube to the left.
On average no current flows through C2421 and thus the voltage across this capacitor remains constant.

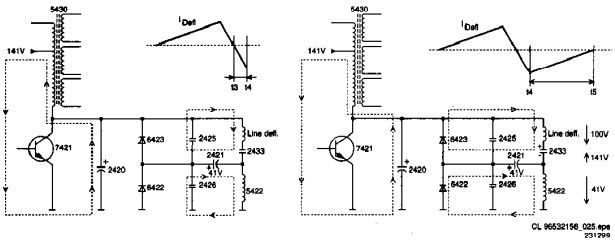

Figure 9-11

Period t3 - t4:
As for the period t2 - t3; but now the current flows in the opposite direction, since the voltage across C2425 and C2426 is higher than the voltage across C2433 and C2421.

Period t4 - t5:
The coils want to maintain the negative current and will charge the capacitors negative. Because of this, D6422 and D6423 will conduct. The voltage is 100 V across the deflection coil and 41 V across L5422. As both diodes conduct, we may consider the voltage to be constant. A linear current flows with the same changing characteristics as in period t1 - t2. The spot now moves from the extreme left of the picture tube to the centre. Before the current becomes zero, and the spot is located in the centre of the frame, TS7421 reverts back into conductivity. First a short negative current will flow. The cycle starts again.

The linearity correction
A constant voltage across the horizontal deflection coil should result in a linear increasing saw-tooth current. This however is not the case as the resistance of the coil is not negligible. In order to compensate for this, a pre-magnetised coil L5421 in series with the deflection coil is used. This coil ensures that during time interval t1 - t3 the circuit-resistance will be higher than during t4 - t5. L5421 is called the linearity coil.
To avoid self-oscillation, R3431 and C2431 are placed parallel to L5421.

The S-correction
Since the sides of the picture are further away from the point of deflection than the centre, a linear saw-tooth current would result in a non-linear image (the centre would be scanned slower than the sides). To solve this, the deflection current for the right- and left side will be reduced.
C2433 is charged quadratic during time interval t1 - t2. Left and right the voltage across the deflection coil decreases, causing the deflection to slow down. In the centre, the voltage increases and the deflection will be faster. An S-shaped current will have to be superimposed onto the saw-tooth current. This correction is called finger-length correction or S-correction. C2433 is relatively small, as a result of which the saw-tooth current will generate a parabolic voltage with negative voltage peaks.. The current also results in a parabolic voltage across C2421, resulting in the finger-length correction, proportionally increasing with the picture width. The EW-DRIVE signal will ensure the largest picture width in the centre of the frame. Here the largest correction is applied. The larger the picture width, the higher the deflection current through C2433.

The E/W-correction
A line, written at the upper- or lower side of the screen, will be larger at the screen centre when a fixed deflection current is used. Therefore the amplitude of the deflection current must be increased when the spot approaches the screen centre. This is called East/West correction.
The EW-DRIVE signal is generated in the HOP and will drive FET TS7480 via TS7481 and optocoupler TS7482. TS7480 will charge capacitor C2423 more or less, increasing the deflection current when reaching the centre of the screen.

Secondary line-voltages
During the blocking time of TS7421, the magnetic energy of coil 1 - 5 of the LOT will be transferred to electrical energy in the secondary winding. Via rectifying and smoothing, the several secondary supply voltages will be generated:
- EHT, Focus and Vg2-voltage
- +180V for the CRT panel (pin 8 LOT)
- +11D for the line deflection (pin 12 LOT)
- +13VLOT for the frame deflection (pin 6 LOT)
- -15VLOT for the frame deflection (pin 3 LOT)
- Filament voltage (pin 9 LOT)

The EHT-INFO signal is derived via R3450//R3451. This signal decreases while the beam current increases. It is fed to the HOP to compensate for loss of picture width and picture height.

The DYN-FASE-CORR signal is fed to the HOP via C2455 and drives a dynamic phase correction necessary because of beam current variations. This is done by regulating T_{ON} of the line transistor TS7421.

East-West circuit
The moment TS7480 is driven into saturation, C2421 will discharge during the flyback. As a consequence of which C2421 must be charged again during the scan via the conduction diode D6422 (as long as C2421 is not charged to the voltage across L5422, D6422 will conduct). The current in the deflection coil is therefore larger than the current flowing in L5422 (1-2). The voltage across the deflection coil increases, so the picture width increases. When TS7480 blocks, C2421 will not discharge anymore and the voltage across C2421 will remain constant. The result is that the voltage across the deflection coil is minimal. The voltage across coil L5422, however, is maximal. This coil (L5422) consists of a transformer:
- As the current through the coil 1-2 increases (smaller picture width), the current through coil 3-4 decreases. Because of the transformer characteristic a higher voltage will be subjected to coil 3-4, which will counteract the current. The current will diminish even further.
- When the current through coil 1-2 diminishes (larger picture width), the current through coil 3-4 increases.

The EW Drive

The EW drive signal originates in the HOP and is supplied to TS7480. The shape of this signal determines the various geometric correction parameters:

- H amplitude
- EW-parabola
- EW-corner
- EW-trapezium
- Horizontal parallelogram
- Horizontal bow

Beam current correction

The EHT-info at point 10 of the LOT is dependent on the value of the beam current and the voltage divider R3450, R3451 and C2450. The EHT-info is fed to the HOP to trim the contrast and to compensate for the changes in picture-width as a function of the EHT-info, when the high-voltage is decreased. The EHT-info is integrated via C2450 and sent to the gate of the E/W FET (TS7480) as a DC-voltage to correct the EW-current.

9.1.11 Vertical (frame) deflection (diagram A4)

Driving the frame output stage

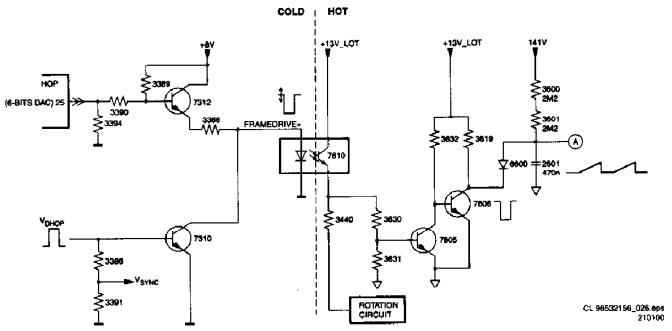

Figure 9-12

The HOP drives the frame output stage. As the HOP is 'cold' and the frame output stage is 'hot', they must be galvanic isolated by means of an optocoupler. In the MG-chassis the HOP generates 3 signals needed for the frame output stage: VDPOS, VDNEG and FRAME ROTATION. To avoid the costs of 3 optocouplers, the frame drive pulse and rotation DC-voltage are added together and then fed to optocoupler TS7610.

This is done as follows: The VD100 signal from the PICNIC (diagram B3 pin 19) is extended for 16.5 lines and inverted via a monostable multivibrator (TS7311 & TS7309, diagram B4). The output signal VDHOP is then superimposed on a DC-voltage from pin 25 of the HOP. The resulting signal is called FRAMEDRIVE+ and is fed to optocoupler 7610 (diagram A4). So this signal contains info for both the frame deflection and the frame rotation.

The circuit around IC7440 will amplify this signal and the output current will flow through the rotation coil. The vertical pulses on this signal are filtered by C2445 to ensure that only a DC-voltage will be supplied to the rotation coil.
The output voltage of the rotation circuit is between -8 and +8 V.

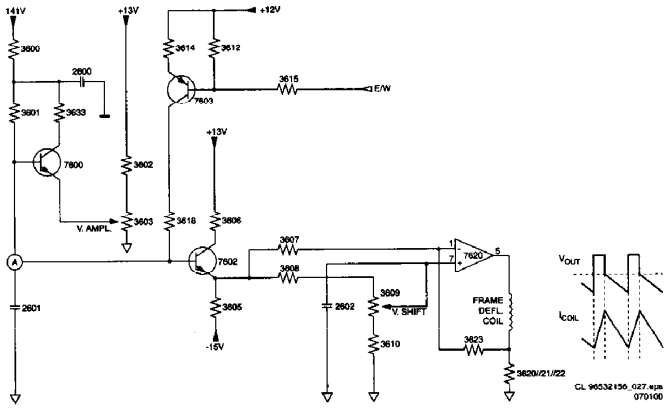

Figure 9-13

The sawtooth voltage for the frame output stage is not generated by the HOP but by a discrete circuit after the optocoupler 7610: via R3600 and R3601 a linear increasing voltage over C2601 is built up with a large time constant.

The circuit around TS7603 is a current source, driving C2601 with a current value derived from the E/W modulator. This will result in an S-shaped voltage on C2601 (also known as EW-correction).

Flyback generator

The frame output stage is supplied via the +13 V and -15 V coming from the LOT. The output of the amplifier is 0 V_{DC}, so a coupling capacitor is not required.

During the (forward) scan, a supply of +13 and -15 V is sufficient to respond to the slow changing current. The flyback generator puts a voltage of -15 V on pin 3. Because of the voltage drop over zenerdiode D6622 (8.2 V), C2622 will be charged to 19 V: being 13 + (15 - 8.2 - 0.7) V.
During the flyback scan, the change in current per time is much larger, so a higher voltage is required. The flyback generator will now generate a voltage of +13 V on pin 3. Added to the charge on C2622 this will give a flyback voltage of 32 V (depending on the CRT size, this value can differ).

The IC amplifier (IC7620, pin 5) supplies the sawtooth current to the frame deflection coil. The current through this coil is measured via R3620//R3621//R3622 and fed back to the inverting input of the amplifier.
R3624 and C2624 on the output of the amplifier, form a filter for high frequencies and in that way also prevents oscillations. Peak voltages on the output, e.g. as a result of a possible flash, are damped by the clamp circuit consisting of D6619, C2627 and R3627. The network consisting of R3625, R3629 and C2629 form an extra damping circuit.

Protection circuit for bridge-coil and frame output stage

The secondary voltage of bridge coil L5422 is guarded at the diode modulator (D6421/22) via a detection circuit consisting of an 8.2 V zenerdiode (diagram A3). When the bridge-coil is working properly, the average voltage on D6422 is such that this zenerdiode will conduct and will drive TS7652 into saturation via the BRIDGE_PROT signal (see diagram A4). When, for any reason, the secondary side of the bridge-coil is shorted, the average voltage on D6422 will drop below the zener-voltage and TS7652 will block. Now capacitor C2642 will be charged. Transistor TS7407 will start conducting and the STANDBY signal will be grounded via R3403. This will switch off the main supply (see diagram A1).

Via the circuit built around TS7641 the frame output stage is guarded. If the frame output stage is working properly, TS7641 and TS7652 will both conduct and thereby discharging C2642. TS7407 is blocked now, causing the STANDBY signal to be high-ohmic.
If there are frame pulses missing, TS7641 will block and capacitor C2642 can be charged. Transistor TS7407 will now start conducting and the STANDBY signal will be grounded via R3403. This will switch off the main supply (see diagram A1).

9.1.12 Audio (diagram B6, A5 & A6)

Introduction
All EM2E sets contain one of ITT's Multistandard Sound Processing IC's for sound decoding. The diversity arises because each member of the MSP-family handles its own set of sound standards:

- MSP3415D: Europe & AP decoding, Stereo incl. NICAM.
- MSP3451G: Global decoding, Virtual Dolby.

This IC takes care of the main FM sound decoding. AM decoding for the L system is done by the HIP. The demodulated L sound is then again source selected and processed in the MSP. The reason for this is the bad AM detection performance of the MSP. In case of NICAM L however, this is handled by the MSP.

All MSP versions contain digital audio processing, used for the basic left/right stereo sound, such as bass, treble, balance, incredible sound and spatial. In addition to that, the MSP3451 is also able to perform Virtual Dolby, a Dolby approved sound mode for surround sound reproduction with left/right speakers only.

Audio source selection
- MSP3515D (stereo)

This IC is an economised version of the MSP3410 that is used in the MG-chassis. It can cover 2 stereo and 1 mono (AM) input. Since more inputs are required, a separate source selector is used (HEF4052, IC7675). This selector has EXT1, EXT2, FRONT and SC1-OUT (Tuner) as input and is connected to the SCART1 input of the MSP3415. The SCART2 input is not used.

Since the MSP3415 has only one SCART output, which is connected to the SCART1, a constant level output and connection to SCART2 is not available. This is fixed by connecting the HEF4052 input selector to the constant level output and to SCART2 via a so-called 'Régimbeau' switch (IC7652).
This switch is needed to prevent feedback (Larsen effect). When EXT2 is chosen as input signal, and the output of SCART2 is selected, this means that the main picture is also EXT2 and will cause the Larsen effect. To prevent this, the record select must be switched to Tuner. This is especially important when decoders are used, behind a 'transparent' VCR connected to EXT2.

To get a constant level output if the Tuner is selected, the SCART1 output (Tuner at any time), has to be fed back to the input selector and selected as input for the MSP (SCART1 input).

The MSP3415 has no separate output to drive a headphone. The headphone is therefore hardwired (on the LSP) to the main sound output.

- MSP3451G (Virtual Dolby)

The MSP3451, which is used in all versions supporting Virtual Dolby, is capable of supporting 4 stereo inputs and 1 mono (AM) INPUT. Therefore the extra input selector (HEF4052) is not needed.

The MSP3451 is also capable of supporting 2 SCART outputs, so the trick used in the MSP3415 set-up to get a constant level output is not needed.

The MSP3451 has a separate headphone output, so sound control be done separate from the speakers.

Audio decoding
At the input a choice can be made between two IF-signals; SIF and SIFM.
The selected signal is fed to the AGC. After this, an ADC converts the IF-signal to digital.

This digital signal can be processed by 2 demodulation channels. The first one is able to handle FM and NICAM signals. The second one can handle FM and AM signals.

Each channel contains a mixer to shift the incoming signal in the frequency domain. This shift is determined by the value of a DCO.

After the down-mix, the signal is fed, via a filter, to a discriminator. From here the AM, FM or NICAM demodulation can be performed.

Both channels contain an 'automatic carrier mute' function, which automatically mutes the output of the analogue section when no carrier is detected.

After demodulation, the FM-signals are subjected to a de-emphasis operation. After that the matrix of the stereo system is applied.

Audio processing
The sound processing in EM2E is completely done by the MSP3415D for 'Stereo' sets or the MSP3451G for 'Virtual Dolby' sets:

- Volume control is done by the user via the SOUND menu.
- Tone control in 'Stereo' sets is done via the BASS/TREBLE control, in 'Virtual Dolby' sets via the 5-band equaliser.
- Headphone control in 'Stereo'-sets is done via the loudspeaker output of the MSP, no sound control possible. In 'Virtual Dolby'-sets, the MSP has a separate Headphone output so separate sound control is possible.
- Mute control can be done in different ways:
  - Via the SOUND_ENABLE line of the OTC. Used during start-up/switch-off conditions, in order to avoid audible plops.
  - Via the decoding part of the MSP.
  - Via the processing part of the MSP.

The mute on the RC or in the UI is per today a combination of processing mute and SOUND_ENABLE line. When a user mute is done, the processing mute will turn down the volume, after which the SOUND_ENABLE line is switched. De-muting is the other way around. The reasons for this is a technical problem with crosstalk of the headphone into the loudspeakers.

Automatic Volume Levelling (AVL)
One of the features of the MSP-family is AVL. If used, it limits the big volume differences in the broadcast between e.g. news transmissions and commercials or within a movie.
To be able to get a Dolby approval (for the Virtual Dolby sets), the AVL feature must be switchable. Therefore, the AVL feature is customer switchable via the menu.

Audio amplification
The audio amplifier part is very straight forward. It uses an integrated power amplifier IC, the TDA2616. It delivers an

output of 2 x 10 WRMS to 2 full range speakers. A subwoofer is not implemented.

The supply voltage is +28 V, generated by the main supply via L5506.

Muting is done via the SOUND-ENABLE line connected to pin 2 of the amplifier-IC and coming from the OTC. This signal is inverted by TS7730, as a result of which at a high level of the SOUND-ENABLE signal, current is sinked from pin 2 and the IC mutes.

9.1.13 Teletext / NexTView (diagram B5)

Teletext

The TXT-decoder in the OTC gets its video signal directly on pin 5 (from the HIP).
The RGB-outputs are available on pins 77/78/79. Fast blanking is realised via pen 80.
In the previous chassis there was separate memory to store the TXT information. In EM2E the DRAM (IC7007) of the microprocessor is also used for the TXT-decoder.

NexTView

NexTView allows the user to display a program guide on the TV screen that contains extensive information for each program.

This information can be displayed in a number of different summaries:

- DAY: The daily summary shows, from the current moment, the program schedule for several stations for a short time ahead.
- CHANNEL: The channel summary shows the program schedule for one station.
- THEME: The theme summary shows, for each theme, the program schedule of the various stations. These themes consist of sport, film, culture, etc. and is determined from the station side.

NexTView does not have to restrict itself to information about the station that is being viewed, but also offers information about other stations. In the various summaries 3 different commands can be given for the various program overviews. These commands appear as follows:

- WATCH: The set immediately switches over to the station concerned.
- REMINDER: The start time and date and the station of the program concerned is stored in the TV reminder list. The TV will give an OSD-message with the program information, or switch on the set at the correct moment (provided the set is in Standby) and tune to the station concerned.
- RECORD: The timer of the video recorder with 'Easylink Plus' is programmed with the data of the program concerned. There has to be a video recorder (with Easylink Plus) connected to SCART2 otherwise the 'RECORD' function will not be highlighted. The connection is via pin 10 from SCART. This means that it has to be a full SCART or at least pin 10 has to be wired.

In order to be able to realise NexTView, two teletext type data flows, Data stream 1 and 2, are transmitted with various sub-code pages of information. This data flow can transport limited information (max. 40 pages). Data stream 1 is quick repeating with a repetition time of approximately 20 to 30 seconds. However, Data stream 2 has a much longer repetition time of approximately half an hour and has a large transport capacity.

- Data stream 1 contains information of the station that is being viewed.
- Data stream 2 contains up to one week of advance information from various stations that are covered by the provider.

9.1.14 CRT / SCAVEM / Rotation (diagram F)

RGB amplifiers

On the CRT panel, the RGB amplifier (TDA6108, IC7307) is located. Via the outputs 9, 8 and 7 the cathodes of the picture tube are driven.
The supply voltage for the amplifier is 180 V and is derived from the LOT.

SCAVEM

The SCAVEM-circuitry is implemented in the layout of the picture tube panel. It is thus not an extra module. SCAVEM means SCAn VElocity Modulation. This means that the horizontal deflection is influenced by the picture content. In an ideal square wave, the sides are limited in slope by a limited bandwidth (5 MHz).
SCAVEM will improve the slope as follows: At a positive slope, a SCAVEM-current is generated which supports the deflection current. The first half of the slope the spot is accelerated and the picture is darker, while at the second half of the slope, the spot is delayed and the slope becomes steeper.
At the end of the slope, the SCAVEM-current decays to zero and the spot is at the original position. An overshoot occurs which improves the impression of sharpness. At the negative slope, the SCAVEM-current counteracts the deflection.
During the first half of the slope, the spot is delayed, the slope becomes steeper.
During the second half the spot accelerates, the SCAVEM-current is zero at the end of the slope.

Via the three resistors R33315, R33317 and R3320, Red, Green and Blue are added together and offered to the emitter TS7300. On the collector of this transistor, configured in a common base, the sum of these 3 signals is obtained. Via the emitter follower formed with TS7301, this signal is conveyed to the differentiator C2303, R3309 and R3318. Only the high frequencies are differentiated (small RC-time).
The positive and negative pulses of this signal drive respectively TS7303 and TS7302 into conductivity. The DC setting of the output stage is set by R3304, R3308, R3316 and R3319. The working voltage of the transistors is settled at half the supply voltage.
At the positive section of the pulse, the current flows through R3318, C2307, the SCAVEM-coil and TS7303. At the negative section of the pulse, the current flows through R3318, C2409, the SCAVEM-coil and TS7302.

Rotation

In sets with a rotation coil (widescreen sets ≥ 32"), the amount of frame rotation is adjusted with the DAC-output of the HOP (see also 'Vertical Deflection').

9.1.15 Software related features

Following features are described:

- Smart Local Doming Prevention (SLDP)
- Auto TV
- Switch ON behaviour

Smart Local Doming Prevention (SLDP)

A CRT with an iron shadow mask shows a considerable amount of local doming (due to local heating), resulting in unwanted colour artefacts.
SLDP helps to reduce these artefacts for both 16:9 and 4:3 sets to an acceptable level. It measures the beam current in areas that are sensitive to local doming and reduces the contrast if the beam current in these places exceeds a pre-set threshold.
The chosen solution in EM2E, is based on the PICNIC hardware and software and it uses the histogram measurement of the PICNIC to make a prediction of the local heating of the CRT shadow mask.

With SLDP, local doming is diminished to an acceptable level at the cost of contrast reduction. By using a 'smart' solution for a part of the necessary contrast reduction, the resulting picture remains even more acceptable.
SLDP is not a feature. It's an algorithm that diminishes local doming effects. These effects occur whenever iron mask (and in a limited way invar mask) tubes are applied. Therefore, there is no reason to make it switchable for the customer. However, SLDP can be switched off via the Service Alignment Mode (SAM).

AutoTV

The AutoTV (or 'Automatic Picture Control' or 'Active Control') aims at giving the customer the best possible picture performance at any time. Therefor it does real time processing of the video signal and as a result, it decides to adapt several video parameters throughout the whole chassis.

The AutoTV feature integrates traditional picture performance, AutoTV functionality and 'smart controls' in order to come to a kind of 'supersmart' TV. It can be subdivided in:

- Auto Noise Reduction. This algorithm measures the amount of noise in the incoming video signal (this is done by the LIMERIC part of the PICNIC). As a result of this measurement, the amount of noise in the picture is corrected, starting from that noise level which is annoying for the customer. Which parameters exactly can be used is depending on the hardware.
- Auto Sharpness. This algorithm measures the amount of sharpness via the bandwidth of the incoming video signal and adapts the peaking frequency in the PICNIC according to this info. If the 'sharpness meter' sees the video content as 'sharp', high frequency peaking will be used. On the other hand, if the picture content is seen as 'not sharp', a low/mid frequency peaking is used. There is a coupling between the Auto Noise and the Auto Sharpness algorithm: if noise is present in the video content, then in general the sharpness will be made less aggressive. Special care has to be taken to the interaction of the LIMERIC and the vertical peaking of the PICNIC: a too big amount of vertical peaking increases the visibility of the 2DNR artefacts.

In the EM2E a limited AutoTV control function is used: only a combination of above described features is used in the background in order to improve the set performance, specially focussed on noise reduction.

Switch ON behaviour

First of all, the microprocessor needs to start up: After the power is applied, the 'Standby supply' starts oscillating, generating the +5V2 and +3V3. When ready, a reset (POR) is generated and the OTC is awakened.

During reset, the OTC puts a high level on all his outputs, causing the degaussing relay to close. After the reset, the outputs and inputs of the OTC must be initialised to their default state. The degaussing output of the OTC must stay high for 12 seconds.

Next step is the check whether the set needs to be in Standby or not. Therefore, the NVM content is read and the Standby-bit is checked. If the set is to stay in Standby, there is no further action.

If the set has to be switched 'on', the Standby-info line is pulled low. This results in the low power mode start-up of the HOP. The line drive starts to run on 50 kHz, wakes up the main supply and the +5 V, +8 V and +141 V supplies become available. The OTC waits until the +8 V is fully present. This is done by checking the ADC input of the OTC. A positive result means three times a positive +8 V detection in a row (time between each polling approx. 5 ms). If this detection still fails after 1 second, an error should be generated and the set must be switched to protection (error: "+8 V).

After detection of the +8 V, the MSP must be reset, since it can disturb I^2C traffic when not properly reset. From this moment on, I^2C traffic is possible.

To be sure that the HOP is properly started up, the POR bit of the HOP should be read. If this is not successful, the Standby info has to be put high again and an error code (code 11: HOP) will be generated. If the reading of the POR bit is successful, the starting procedure can be continued.

The Standby info line must be switched high again. The sync mode and the black current stabilisation loop of the HOP must be disabled in order to have a smooth start-up. Within 23.5 ms after reading the HOP POR bit, the HOP has to be started up via the HOP_start commando. If this condition is not fulfilled, the HOP will stop his line drive again and the set will not be able to start up.

During start-up of the deflection, I^2C traffic must be disabled for 250 ms to avoid data corruption. If flashes or spikes are generated during EHT start-up, I^2C data could be disturbed or corrupted.

After deflection is powered up completely, all protection algorithms are set active.
The rest of the NVM content can now be read and the IC's can be initialised according this info.

If SLDP is present in the set, an initialisation of SLDP has to be performed, including a calibration of the beamcurrent ADC.

The sync-mode of the HOP must be switched to active and the black current stabilisation loop in the HOP is switched on. Some extra checking is done to ensure that the loops are completely stabilised. Software sets all the necessary parameters for a correct sound and image and unblanks the picture.

A provision is foreseen to avoid sets in the field that will never unblank, if the picture tube is severely worn out. If the black current stabilisation does not become stable within a time frame of 30 seconds, the picture is unblanked anyway